DOCUMENT NUMBER AND REVISION

VL-FS-MGLS24064-21C REV. A

(MGLS24064-HT-LED04YG-SCH C)

DOCUMENT TITLE:

SPECIFICATION

OF

LCD MODULE TYPE

ITEM NO.: MGLS24064-21C

DEPARTMENT	NAME	SIGNATURE	DATE
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VARITRONIX LIMITED

Specification
of
LCD Module Type
Item No.: MGLS24064-21C

1. General Description

- 240 x 64 dots STN Positive Yellow Transflective LCD graphic module.
- Driving scheme: 1/64 duty, 1/8.7 bias.
- Viewing direction: 6 O'clock.
- 'TOSHIBA' T6963C-0101 flat pack or equivalent LCD controller.
- 'TOSHIBA' T6A39 flat pack or equivalent LCD segment drivers.
- 'TOSHIBA' T6A40 flat pack or equivalent LCD common driver.
- 8K byte display SRAM.
- Yellow-green LED04 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	180.0(W) x 65.0(H) x 16.0 MAX.(D)	mm
Viewing area	132.0(W) x 39.0(H)	mm
Active area	127.15(W) x 33.87(H)	mm
Display format	240(W) x 64(H)	dots
Dot size	0.48(H) x 0.48(W)	mm
Dot spacing	0.05(H) x 0.05(W)	mm
Dot pitch	0.53(H) x 0.53(W)	mm
Weight:	Approx. 157	grams

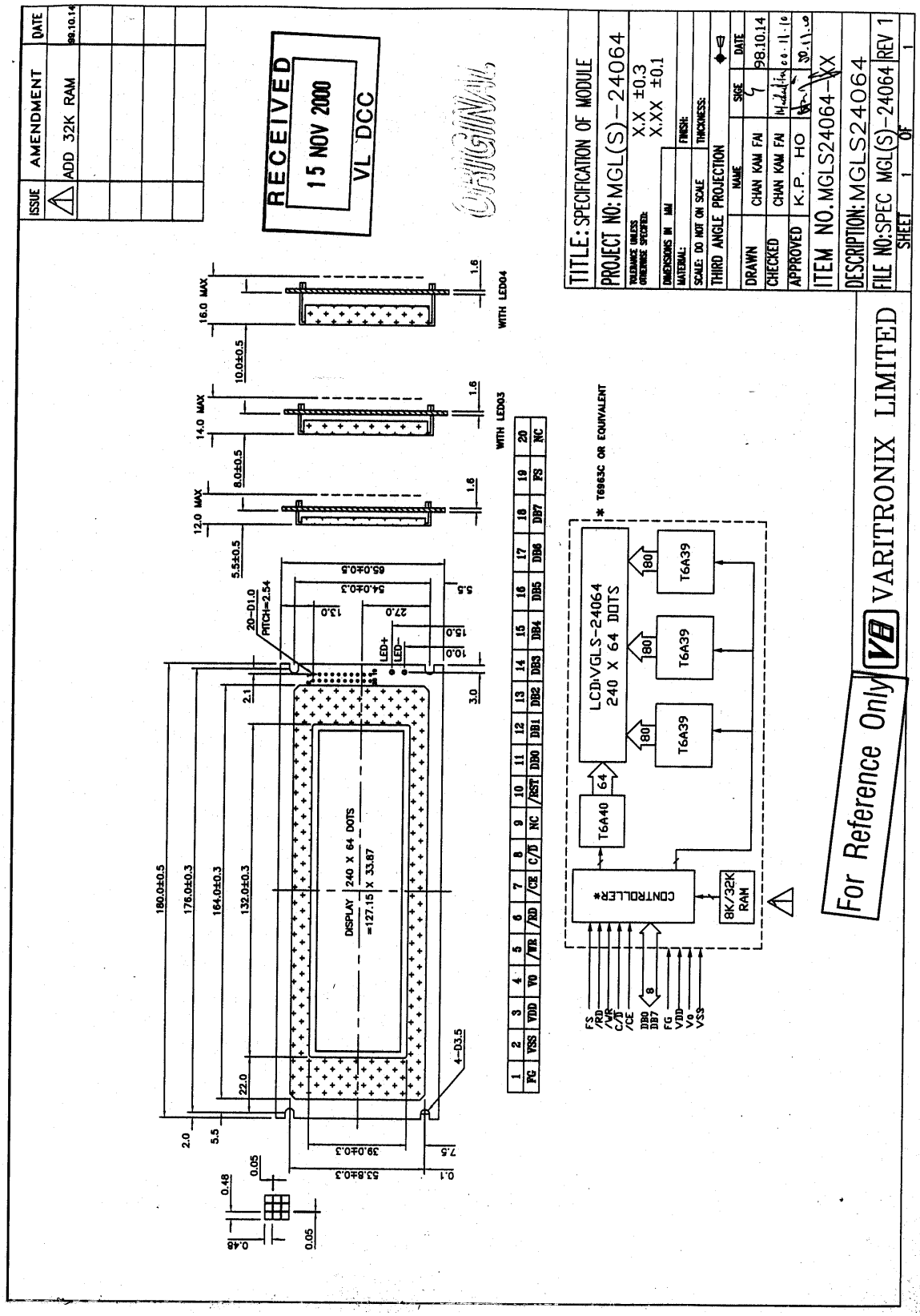

Figure 1: Module Specification

3. Interface signals

Table 2

Pin No.	Symbol	Description
1	FG	Frame ground (see note 1)
2	VSS	Ground
3	VDD	Power supply for logic (+5V)
4	V0	Power supply for LCD drive
5	/WR	Data write. Write data to controller T6963C when “L”.
6	/RD	Data read. Read data from controller T6963C when “L”.
7	/CE	Chip enable of controller when ”L”.
8	C/$\overline{D}$	Command/Data read/write. “H” for command read/write and “L” for data read/write.
9	NC	Not connected
10	/RST	Controller reset when “L”.
11	DB0	Data input/output (LSB)
12	DB1	Data input/output
13	DB2	Data input/output
14	DB3	Data input/output
15	DB4	Data input/output
16	DB5	Data input/output
17	DB6	Data input/output
18	DB7	Data input/output (MSB)
19	FS	Font select. ”H” for 6 x 8 font & ”L” for 8 x 8 font
20	NC	Not connected

Note 1: This pin is electrically connected to the metal bezel(frame).
User can choose to connect this pin to VSS or leave it open.

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings(Ta = 25 ºC)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Supply voltage (LCD drive)	VLCD=VDD – V0	-0.3	+28.0	V
Input voltage	Vin	-0.3	VDD +3.0	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	+70°C	-30°C	+80°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 5V±5%,VSS = 0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		4.75	5.0	5.25	V
Supply voltage (LCD)	VLCD =VDD-V0	VDD = 5V, Note 1	13.6	14.6	15.6	V
Input signal voltage	VIN	"H" level	VDD-2.2	-	VDD	V
		"L" level	0	-	0.8	V
Supply current (Logic & LCD)	IDD	Character mode	-	8	12	mA
Supply current (LCD)	I0	Character mode, Note 1	-	3.3	5	mA
Supply voltage of yellow-green LED04 backlight	VLED	Forward current =630mA Number of LED dies =126	3.9	4.1	4.3	V

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

At Ta = -20°C To +70°C, VDD = 5V±5%,VSS=0V

Refer to Fig. 2, the bus timing diagram.

Table 6

Parameter	Symbol	Min.	Max.	Unit
C/$\overline{D}$ Set-up time	t_{CDS}	100	-	ns
C/$\overline{D}$ Hold Time	t_{CDH}	10	-	ns
/CE,/RD,/WR Pulse Width	t_{CE}, t_{RD}, t_{WR}	80	-	ns
Data Set-up Time	t_{DS}	80	-	ns
Data Hold Time	t_{DH}	40	-	ns
Access Time	t_{ACC}	-	150	ns
Output Hold Time	t_{OH}	10	50	ns

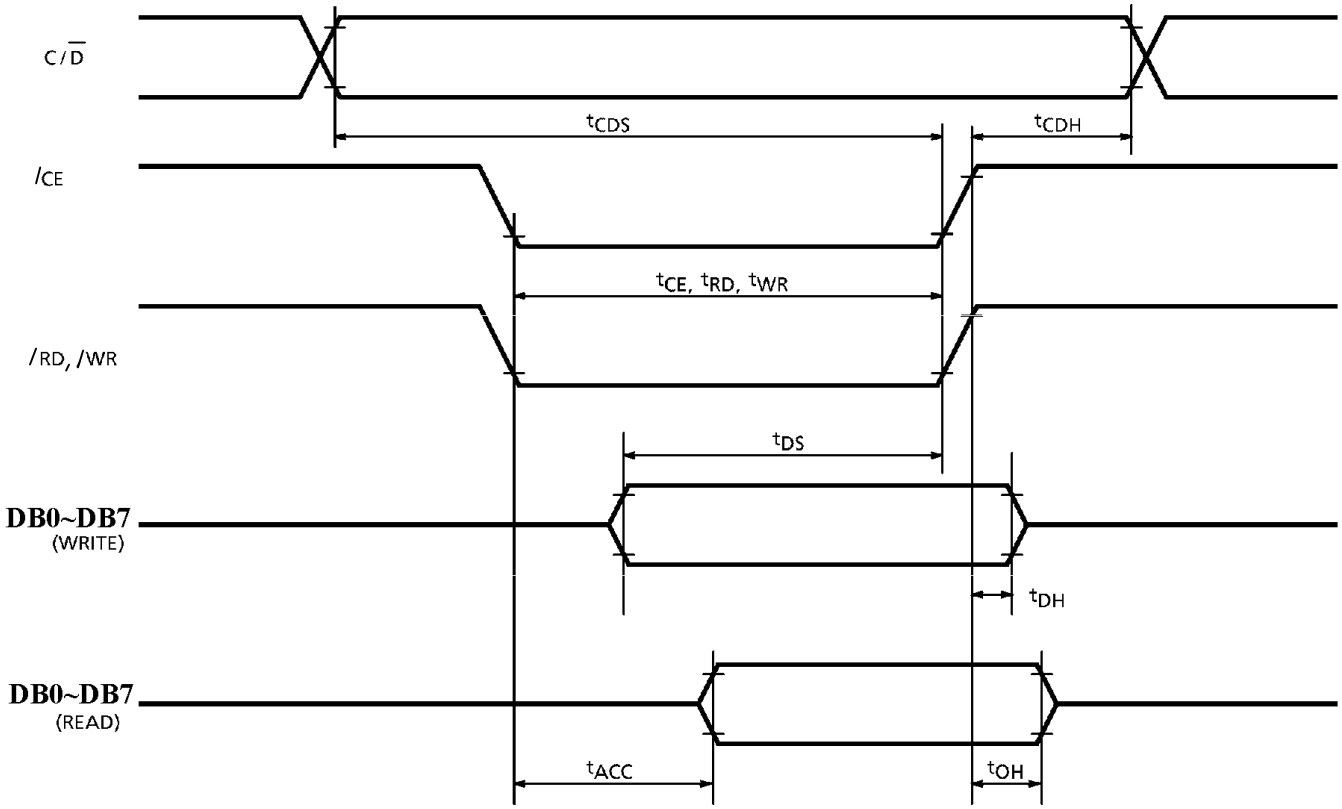

Figure 2: Bus Timing Diagram

5.3 Timing Diagram of VDD Against V0.

Power on sequence shall meet the requirement of Figure 3, the timing diagram of VDD against V0.

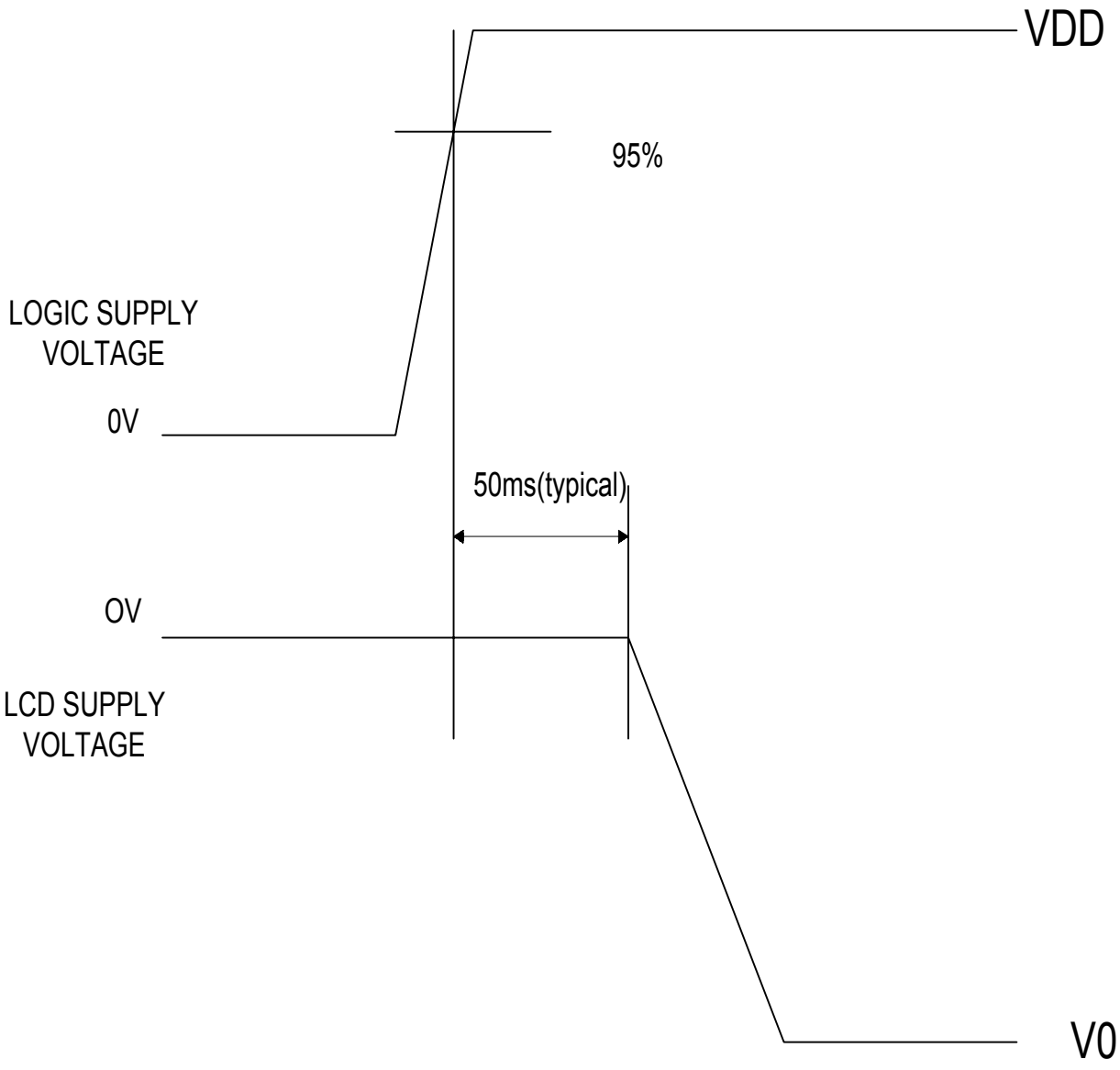

Figure 3: Timing Diagram of VDD Against V0.

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