- **Low Supply-Voltage Range, 1.8 V . . . 3.6 V**
- **Ultralow-Power Consumption:**
  - **Active Mode: 160 µA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.9 µA**
  - **Off Mode (RAM Retention) : 0.1 µA**
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in 6 µs**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **16-Bit Timer_B With Three Capture/Compare-With-Shadow Registers**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **On-Chip Comparator**
- **Serial Communication Interface (USART), Software Selects Asynchronous UART or Synchronous SPI**
- **Programmable Code Protection With Security Fuse**
- **Family Members Include:**
  - **MSP430C1331: 8KB ROM, 256B RAM**
  - **MSP430C1351: 16KB ROM, 512B RAM**
- **Available in 64-Pin Quad Flat Pack (QFP)**
- **Emulation: Use MSP430F13xIPM**
- **For Complete Module Descriptions, See the *MSP430x1xx Family User's Guide*, Literature Number SLAU049**

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 µs.

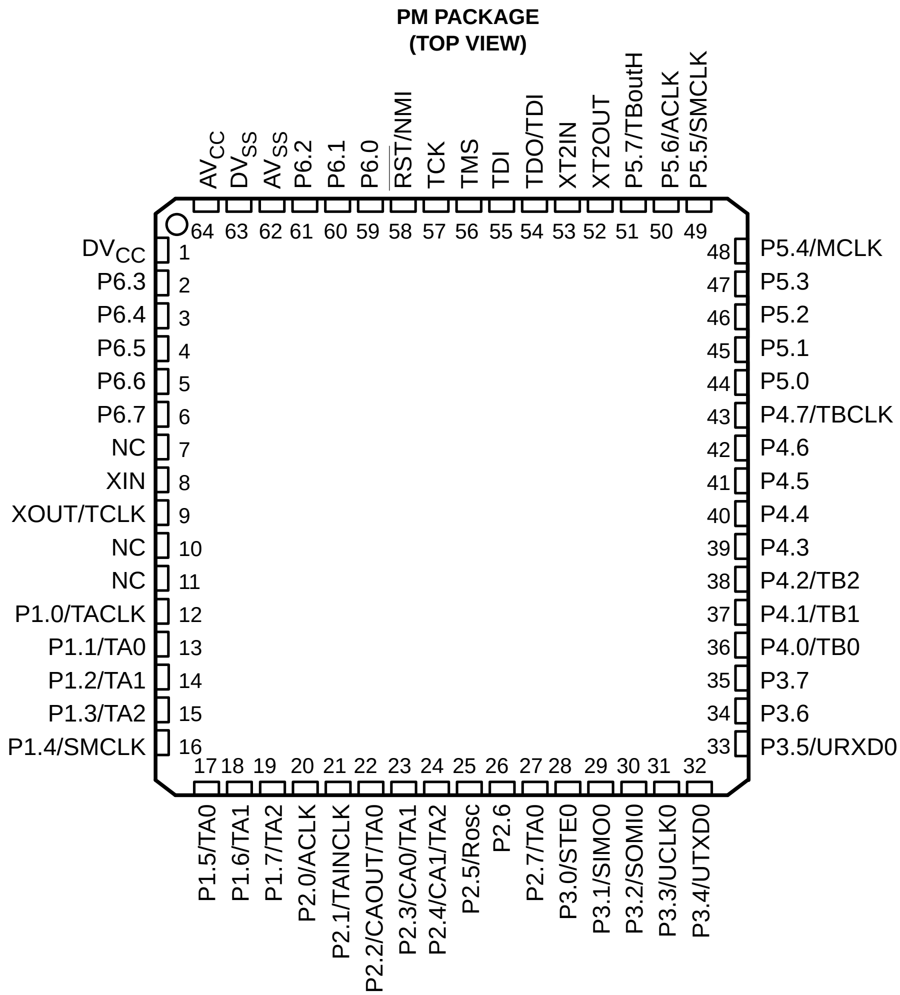
The MSP430C13x1 is a microcontroller configuration with two built-in 16-bit timers, one universal serial synchronous/asynchronous communication interfaces (USART), and 48 I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and process and transmit the data to a host system. The timers make the configurations ideal for industrial control applications, hand-held meters, etc.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	PLASTIC 64-PIN QFP (PM)
–40°C to 85°C	MSP430C1331IPM MSP430C1351IPM

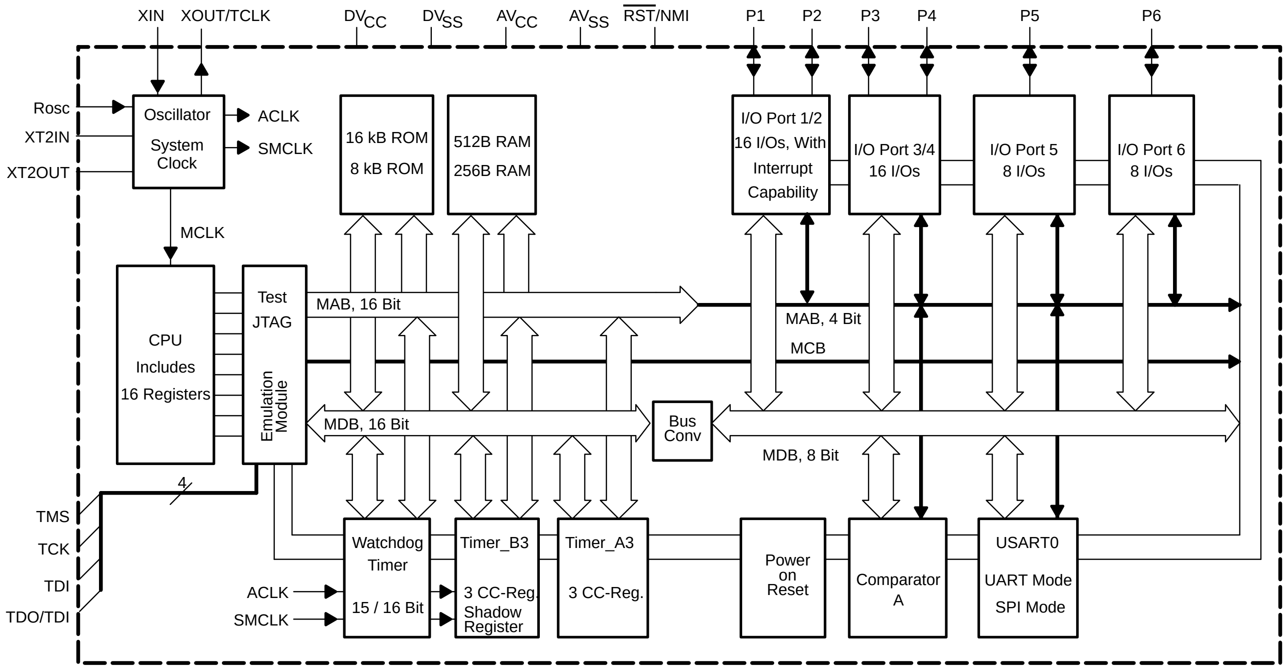
pin designation, MSP430C1331, MSP430C1351



NC – No internal connection

functional block diagrams

MSP430C13x1



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AV_{CC}	64		Supply voltage, positive terminal. AV_{CC} and DV_{CC} are internally connected together.
AV_{SS}	62		Supply voltage, negative terminal. AV_{SS} and DV_{SS} are internally connected together.
DV_{CC}	1		Supply voltage, positive terminal. AV_{CC} and DV_{CC} are internally connected together.
DV_{SS}	63		Supply voltage, negative terminal. AV_{SS} and DV_{SS} are internally connected together.
P1.0/TACLK	12	I/O	General digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	13	I/O	General digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output
P1.2/TA1	14	I/O	General digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General digital I/O pin/SMCLK signal output
P1.5/TA0	17	I/O	General digital I/O pin/Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General digital I/O pin/Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General digital I/O pin/Timer_A, compare: Out2 output/
P2.0/ACLK	20	I/O	General digital I/O pin/ACLK output
P2.1/TAINCLK	21	I/O	General digital I/O pin/Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	22	I/O	General digital I/O pin/Timer_A, capture: CCI0B input/Comparator_A output
P2.3/CA0/TA1	23	I/O	General digital I/O pin/Timer_A, compare: Out1 output/Comparator_A input
P2.4/CA1/TA2	24	I/O	General digital I/O pin/Timer_A, compare: Out2 output/Comparator_A input
P2.5/Rosc	25	I/O	General-purpose digital I/O pin, input for external resistor defining the DCO nominal frequency
P2.6	26	I/O	General digital I/O pin
P2.7/TA0	27	I/O	General digital I/O pin/Timer_A, compare: Out0 output
P3.0/STE0	28	I/O	General digital I/O, slave transmit enable – USART0/SPI mode

Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
P3.1/SIMO0	29	I/O	General digital I/O, slave in/master out of USART0/SPI mode
P3.2/SOMI0	30	I/O	General digital I/O, slave out/master in of USART0/SPI mode
P3.3/UCLK0	31	I/O	General digital I/O, external clock input – USART0/UART or SPI mode, clock output – USART0/SPI mode
P3.4/UTXD0	32	I/O	General digital I/O, transmit data out – USART0/UART mode
P3.5/URXD0	33	I/O	General digital I/O, receive data in – USART0/UART mode
P3.6	34	I/O	General digital I/O
P3.7	35	I/O	General digital I/O
P4.0/TB0	36	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR0
P4.1/TB1	37	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR1
P4.2/TB2	38	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR2
P4.3	39	I/O	General-purpose digital I/O
P4.4	40	I/O	General-purpose digital I/O
P4.5	41	I/O	General-purpose digital I/O
P4.6	42	I/O	General-purpose digital I/O
P4.7/TBCLK	43	I/O	General-purpose digital I/O, input clock TBCLK – Timer_B7
P5.0	44	I/O	General-purpose digital I/O
P5.1	45	I/O	General-purpose digital I/O
P5.2	46	I/O	General-purpose digital I/O
P5.3	47	I/O	General-purpose digital I/O
P5.4/MCLK	48	I/O	General-purpose digital I/O, main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O, submain system clock SMCLK output
P5.6/ACLK	50	I/O	General-purpose digital I/O, auxiliary clock ACLK output
P5.7/TBoutH	51	I/O	General-purpose digital I/O, switch all PWM digital output ports to high impedance – Timer_B7 TB0 to TB2
P6.0	59	I/O	General digital I/O
P6.1	60	I/O	General digital I/O
P6.2	61	I/O	General digital I/O
P6.3	2	I/O	General digital I/O
P6.4	3	I/O	General digital I/O
P6.5	4	I/O	General digital I/O
P6.6	5	I/O	General digital I/O
P6.7	6	I/O	General digital I/O
$\overline{RST}$/NMI	58	I	Reset input, nonmaskable interrupt input port
TCK	57	I	Test clock. TCK is the clock input port for device programming test.
TDI	55	I	Test data input. TDI is used as a data input port. The device protection fuse is connected to TDI.
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output
TMS	56	I	Test mode select. TMS is used as an input port for device test.
NC	7, 10, 11		No internal connection
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT/TCLK	9	I/O	Output terminal of crystal oscillator XT1 or test clock input
XT2IN	53	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
XT2OUT	52	O	Output terminal of crystal oscillator XT2

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 ––> R5
Single operands, destination only	e.g. CALL R8	PC ––>(TOS), R8––> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 ––> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)––> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) ––> M(TONI)
Absolute	✓	✓	MOV and MEM,and TCDAT		M(MEM) ––> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) ––> M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) ––> R11 R10 + 2––> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 ––> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 1 (LPM1);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
    DCO’s dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2);
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO’s dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3);
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO’s dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4);
  - CPU is disabled
    ACLK is disabled
    MCLK and SMCLK are disabled
    DCO’s dc-generator is disabled
    Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh – 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog	WDTIFG (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator fault	NMIIFG (see Notes 1 & 4) OFIFG (see Notes 1 & 4)	(Non)maskable (Non)maskable	0FFFCh	14
Timer_B3	TBCCR0 CCIFG (see Note 2)	Maskable	0FFFAh	13
Timer_B3	TBCCR1 and TBCCR2 CCIFGs, TBIFG (see Notes 1 & 2)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF6h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
USART0 receive	URXIFG0	Maskable	0FFF2h	9
USART0 transmit	UTXIFG0	Maskable	0FFF0h	8
			0FFEEh	7
Timer_A3	TACCR0 CCIFG (see Note 2)	Maskable	0FFECh	6
Timer_A3	TACCR1 and TACCR2 CCIFGs, TAIFG (see Notes 1 & 2)	Maskable	0FFEAh	5
I/O port P1 (eight flags)	P1IFG.0 (see Notes 1 & 2) To P1IFG.7 (see Notes 1 & 2)	Maskable	0FFE8h	4
			0FFE6h	3
			0FFE4h	2
I/O port P2 (eight flags)	P2IFG.0 (see Notes 1 & 2) To P2IFG.7 (see Notes 1 & 2)	Maskable	0FFE2h	1
			0FFE0h	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. Nonmaskable: neither the individual nor the general interrupt-enable bit will disable an interrupt event.
4. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable can not disable it.

special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address 0h

7	6	5	4	3	2	1	0
UTXIE0	URXIE0		NMIIE			OFIE	WDTIE
rw-0	rw-0		rw-0			rw-0	rw-0

WDTIE: Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.

OFIE: Oscillator-fault-interrupt enable

NMIIE: Nonmaskable-interrupt enable

URXIE0: USART0, UART, and SPI receive-interrupt enable

UTXIE0: USART0, UART, and SPI transmit-interrupt enable

Address 01h

7	6	5	4	3	2	1	0

interrupt flag register 1 and 2

Address 02h

7	6	5	4	3	2	1	0
UTXIFG0	URXIFG0		NMIIFG			OFIFG	WDTIFG
rw-1	rw-0		rw-0			rw-1	rw-0

WDTIFG: Set on Watchdog Timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-up or a reset condition at $\overline{\text{RST}}$/NMI pin in reset mode.

OFIFG: Flag set on oscillator fault

NMIIFG: Set via $\overline{\text{RST}}$/NMI pin

URXIFG0: USART0, UART, and SPI receive flag

UTXIFG0: USART0, UART, and SPI transmit flag

Address 03h

7	6	5	4	3	2	1	0

module enable registers 1 and 2

Address 04h

7	6	5	4	3	2	1	0
UTXE0	URXE0 USPIE0						
rw-0	rw-0						

URXE0: USART0, UART receive enable

UTXE0: USART0, UART transmit enable

USPIE0: USART0, SPI (synchronous peripheral interface) transmit and receive enable

Address 05h

7	6	5	4	3	2	1	0

Legend:
- **rw:** Bit Can Be Read and Written
- **rw-0:** Bit Can Be Read and Written. It Is Reset by PUC.
- (shaded box): SFR Bit Not Present in Device

memory organization

		MSP430C1331	MSP430C1351
Memory Interrupt vector Code memory	Size ROM ROM	8kB 0FFFFh – 0FFE0h 0FFFFh – 0E000h	16kB 0FFFFh – 0FFE0h 0FFFFh – 0C000h
RAM	Size	256 Byte 02FFh – 0200h	512 Byte 03FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions.

digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

oscillator and system clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

USART0

The MSP430C13x1 devices have one hardware universal synchronous/asynchronous receive transmit (USART0) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

timer_B3

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

comparator_A

The primary function of the comparator_A module is to support precision slope analog–to–digital conversions, battery–voltage supervision, and monitoring of external analog signals.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog Timer control	WDTCTL	0120h
Timer_B3	Timer_B interrupt vector	TBIV	011Eh
	Timer_B control	TBCTL	0180h
	Capture/compare control 0	TBCCTL0	0182h
	Capture/compare control 1	TBCCTL1	0184h
	Capture/compare control 2	TBCCTL2	0186h
	Reserved		0188h
	Reserved		018Ah
	Reserved		018Ch
	Reserved		018Eh
	Timer_B register	TBR	0190h
	Capture/compare register 0	TBCCR0	0192h
	Capture/compare register 1	TBCCR1	0194h
	Capture/compare register 2	TBCCR2	0196h
	Reserved		0198h
	Reserved		019Ah
	Reserved		019Ch
	Reserved		019Eh
Timer_A3	Timer_A interrupt vector	TAIV	012Eh
	Timer_A control	TACTL	0160h
	Capture/compare control 0	TACCTL0	0162h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 2	TACCTL2	0166h
	Reserved		0168h
	Reserved		016Ah
	Reserved		016Ch
	Reserved		016Eh
	Timer_A register	TAR	0170h
	Capture/compare register 0	TACCR0	0172h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 2	TACCR2	0176h
	Reserved		0178h
	Reserved		017Ah
	Reserved		017Ch
	Reserved		017Eh
PERIPHERALS WITH BYTE ACCESS			
USART0	Transmit buffer	U0TXBUF	077h
	Receive buffer	U0RXBUF	076h
	Baud rate	U0BR1	075h
	Baud rate	U0BR0	074h
	Modulation control	U0MCTL	073h
	Receive control	U0RCTL	072h
	Transmit control	U0TCTL	071h
	USART control	U0CTL	070h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control2	CACTL2	05Ah
	Comparator_A control1	CACTL1	059h
Basic Clock	Basic clock system control2	BCSCTL2	058h
	Basic clock system control1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS} . . . . –0.3 V to + 4.1 V
Voltage applied to any pin (referenced to V_{SS}) . . . . –0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . ±2 mA
Storage temperature (unprogrammed device) . . . . −55°C to 150°C
Storage temperature (programmed device) . . . . −40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}.

PARAMETER			MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$)			1.8		3.6	V
Supply voltage, V_{SS} ($AV_{SS} = DV_{SS} = V_{SS}$)			0.0		0.0	V
Operating free-air temperature range, T_A			–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Notes 1 and 2)	LF selected, XTS=0	Watch crystal		32768		Hz
	XT1 selected, XTS=1	Ceramic resonator	450		8000	kHz
	XT1 selected, XTS=1	Crystal	1000		8000	kHz
XT2 crystal frequency, $f_{(XT2)}$		Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	
Low-level input voltage (TCK, TMS, TDI, RST/NMI), V_{IL} (excluding Xin, Xout)		V_{CC} = 2.2 V/3 V	V_{SS}		V_{SS} +0.6	V
High-level input voltage (TCK, TMS, TDI, RST/NMI), V_{IH} (excluding Xin, Xout)		V_{CC} = 2.2 V/3 V	0.8×V_{CC}		V_{CC}	V
Input levels at Xin and Xout	$V_{IL(Xin, Xout)}$	V_{CC} = 2.2 V/3 V	V_{SS}		0.2×V_{CC}	V
	$V_{IH(Xin, Xout)}$		0.8×V_{CC}		V_{CC}	

NOTES: 1. In LF mode, the LFXT1 oscillator requires a watch crystal and the LFXT1 oscillator requires a 5.1-MΩ resistor from XOUT to V_{SS} when V_{CC} < 2.5 V. In XT1 mode, the LFXT1. and XT2 oscillators accept a ceramic resonator or a 4-MHz crystal frequency at V_{CC} ≥ 2.2 V. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or an 8-MHz crystal frequency at V_{CC} ≥ 2.8 V.
2. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, FXT1 accepts a ceramic resonator or a crystal.

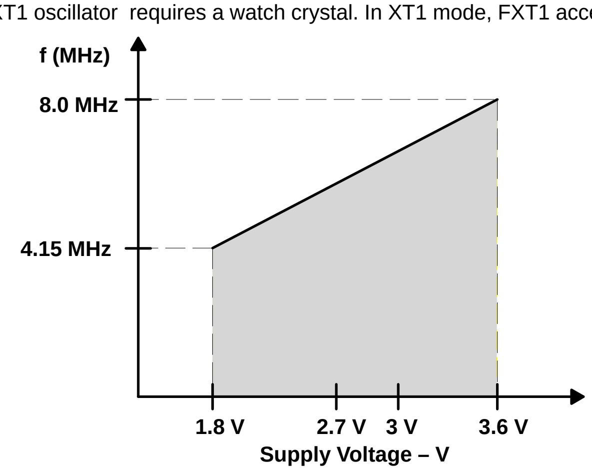


Figure 1. Frequency vs Supply Voltage

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz, XTS=0, SELM=(0,1)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		160	200	μA
			V_{CC} = 3 V		240	300	
	Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)}$ = 4 096 Hz, $f_{(ACLK)}$ = 4,096 Hz XTS=0, SELM=(0,1), XTS=0, SELM=3	T_A = –40°C to 85°C	V_{CC} = 2.2 V		2.5	7	μA
			V_{CC} = 3 V		2.5	7	
$I_{(LPM0)}$	Low-power mode, (LPM0) (see Note 1)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		32	45	μA
			V_{CC} = 3 V		55	70	
$I_{(LPM2)}$	Low-power mode, (LPM2), f(MCLK) = f (SMCLK) = 0 MHz, f(ACLK) = 32.768 Hz, SCG0 = 0	T_A = –40°C to 85°C	V_{CC} = 2.2 V		11	14	μA
			V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 (see Note 2)	T_A = –40°C	V_{CC} = 2.2 V		0.8	1.5	μA
		T_A = 25°C			0.9	1.5	
		T_A = 85°C			1.6	2.8	
		T_A = –40°C	V_{CC} = 3 V		1.8	2.2	μA
		T_A = 25°C			1.8	2.2	
		T_A = 85°C			2.3	3.9	
$I_{(LPM4)}$	Low-power mode, (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1	T_A = –40°C	V_{CC} = 2.2 V		0.1	0.5	μA
		T_A = 25°C			0.1	0.5	
		T_A = 85°C			0.8	2.5	
		T_A = –40°C	V_{CC} = 3 V		0.1	0.5	μA
		T_A = 25°C			0.1	0.5	
		T_A = 85°C			0.8	2.5	

NOTES: 1. Timer_B is clocked by f(DCOCLK) = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
2. Timer_B is clocked by f(ACLK) = 32,768 Hz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. The current consumption in LPM2 and LPM3 are measured with ACLK selected.

Current consumption of active mode versus system frequency

$$I(AM) = I(AM)\,[1\text{ MHz}] \times f(System)\,[\text{MHz}]$$

Current consumption of active mode versus supply voltage

$$I_{(AM)} = I_{(AM)\,[3\text{ V}]} + 175\ \mu A/V \times (V_{CC} - 3\text{ V})$$

SCHMITT-trigger inputs – Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.5	V
		V_{CC} = 3 V	1.5		1.9	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.90		1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.4		1	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

standard inputs – $\overline{RST}$/NMI; JTAG: TCK, TMS, TDI, TDO/TDI

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	V_{CC} = 2.2 V / 3 V	V_{SS}		V_{SS}+0.6	V
V_{IH}	High-level input voltage		0.8×V_{CC}		V_{CC}	V

outputs – Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{CC}–0.25		V_{CC}	V
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{CC}–0.6		V_{CC}	
		$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{CC}–0.25		V_{CC}	
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 3 V,	See Note 2	V_{CC}–0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

outputs – Ports P1, P2, P3, P4, P5, and P6 (continued)

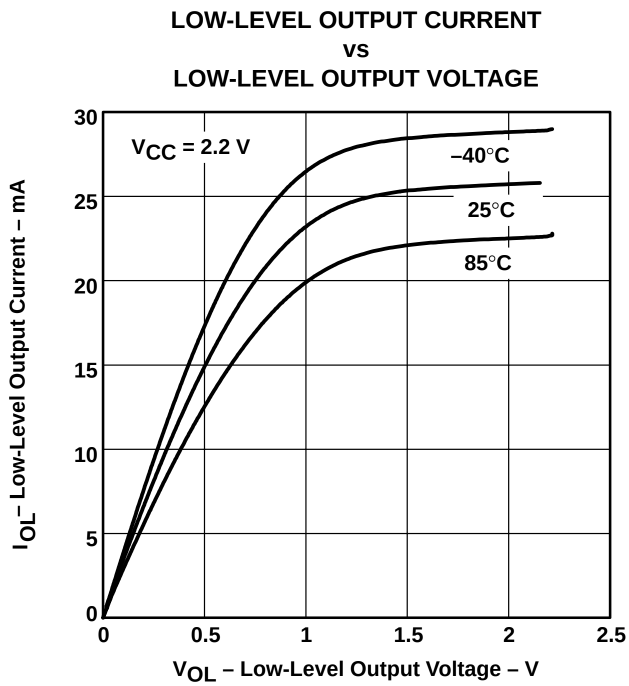


Figure 2

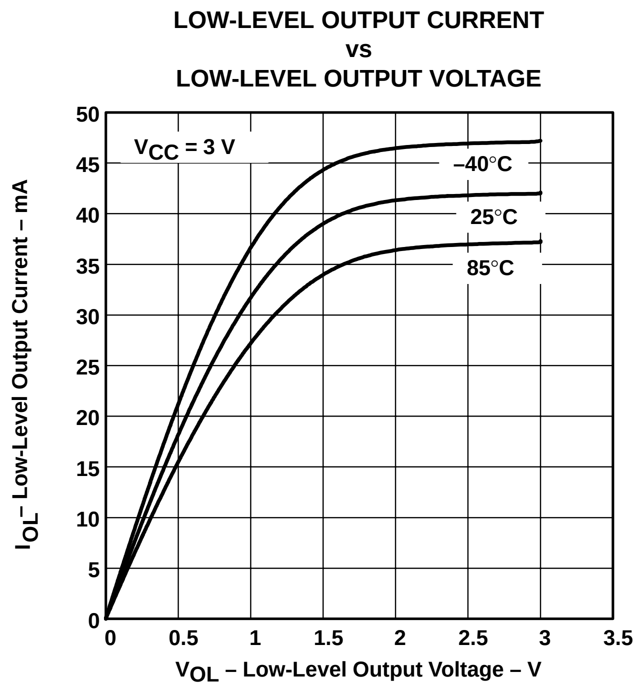


Figure 3

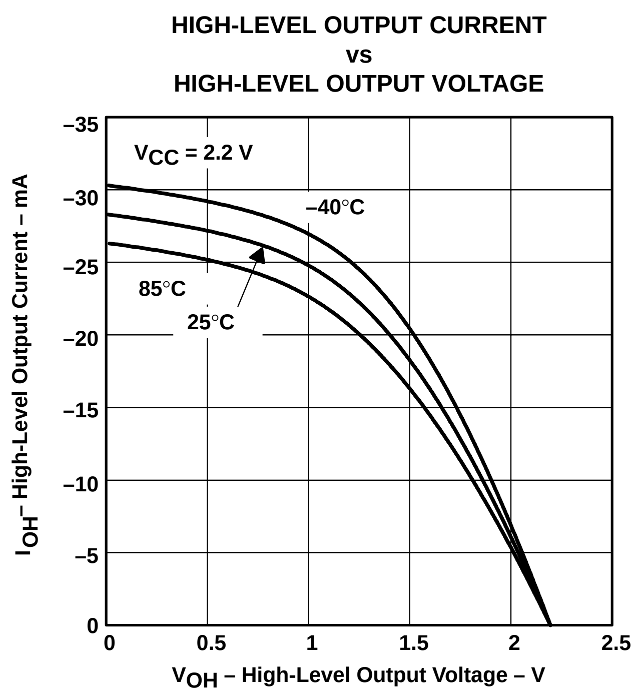


Figure 4

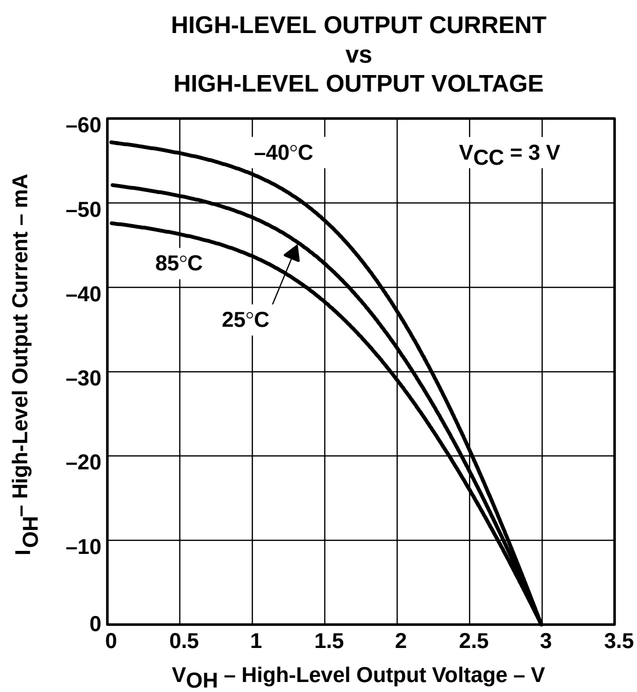


Figure 5

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

input frequency – Ports P1, P2, P3, P4, P5, and P6

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(IN)}$	$t_{(h)} = t_{(L)}$	V_{CC} = 2.2 V			8	MHz
		V_{CC} = 3 V			10	

capture timing _ Timer_A3: TA0, TA1, TA2; Timer_B3: TB0, TB1, TB2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(int)}$	Ports P2, P4: External trigger signal for the interrupt flag (see Notes 1 and 2)	V_{CC} = 2.2 V/3 V	1.5			Cycle
		V_{CC} = 2.2 V	62			ns
		V_{CC} = 3 V	50			

NOTES: 1. The external signal sets the interrupt flag every time $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$. The conditions to set the flag must be met independently of this timing constraint. $t_{(int)}$ is defined in MCLK cycles.
2. The external signal needs additional timing because of the maximum input-frequency constraint.

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{TAx}, f_{TBx}	TA0..2, TB0..2 Internal clock source, SMCLK signal applied (see Note 1)	C_L = 20 pF		DC		f_{System}	MHz
f_{ACLK}, f_{MCLK}, f_{SMCLK}	P5.6/ACLK, P5.4/MCLK, P5.5/SMCLK	C_L = 20 pF				f_{System}	
t_{Xdc}	Duty cycle of output frequency	P2.0/ACLK C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{ACLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{ACLK} = f_{LFXT1} = f_{LF}$	30%		70%	
			$f_{ACLK} = f_{LFXT1/n}$		50%		
		P1.4/SMCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{SMCLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{SMCLK} = f_{LFXT1} = f_{LF}$	35%		65%	
			$f_{SMCLK} = f_{LFXT1/n}$	50%– 15 ns	50%	50%– 15 ns	
			$f_{SMCLK} = f_{DCOCLK}$	50%– 15 ns	50%	50%– 15 ns	

NOTE 1: The limits of the system clock MCLK has to be met; the system (MCLK) frequency should not exceed the limits. MCLK and SMCLK frequencies can be different.

external interrupt timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(int)}$	Ports P1, P2: External trigger signal for the interrupt flag (see Notes 1 and 2)	V_{CC} = 2.2 V/3 V	1.5			Cycle
		V_{CC} = 2.2 V	62			ns
		V_{CC} = 3 V	50			

NOTES: 1. The external signal sets the interrupt flag every time $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$. The conditions to set the flag must be met independently of this timing constraint. $t_{(int)}$ is defined in MCLK cycles.
2. The external signal needs additional timing because of the maximum input-frequency constraint.

wake-up LPM3

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V/3 V			6	µs
		f = 2 MHz				6	
		f = 3 MHz				6	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

leakage current (see Note 1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(P1.x)}$	Leakage current	Port P1	Port 1: $V_{(P1.x)}$ (see Note 2)	V_{CC} = 2.2 V/3 V			±50	nA
$I_{lkg(P2.x)}$		Port P2	Port 2: $V_{(P2.3)}$ $V_{(P2.4)}$ (see Note 2)				±50	

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input and there must be no optional pullup or pulldown resistor.

RAM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRAMh	CPU HALTED (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

Comparator_A (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON=1, CARSEL=0, CAREF=0	V_{CC} = 2.2 V		30	47	µA
			V_{CC} = 3 V		55	74	
$I_{(Refladder/Refdiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V		40	57	µA
			V_{CC} = 3 V		60	87	
$V_{(IC)}$	Common-mode input voltage	CAON =1	V_{CC} = 2.2 V/3 V	0		V_{CC}–1	V
$V_{(Ref025)}$ See Figure 6	$\frac{\text{Voltage at 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2, See Figure 6	V_{CC} = 2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$ See Figure 6	$\frac{\text{Voltage at 0.5} V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2, See Figure 6	V_{CC} = 2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$		PCA0=1, CARSEL=1, CAREF=3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2 T_A = 85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3 V	400	490	550	
$V_{(offset)}$	Offset voltage	See Note 2	V_{CC} = 2.2 V/3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON=1	V_{CC} = 2.2 V/3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF=0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF=1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

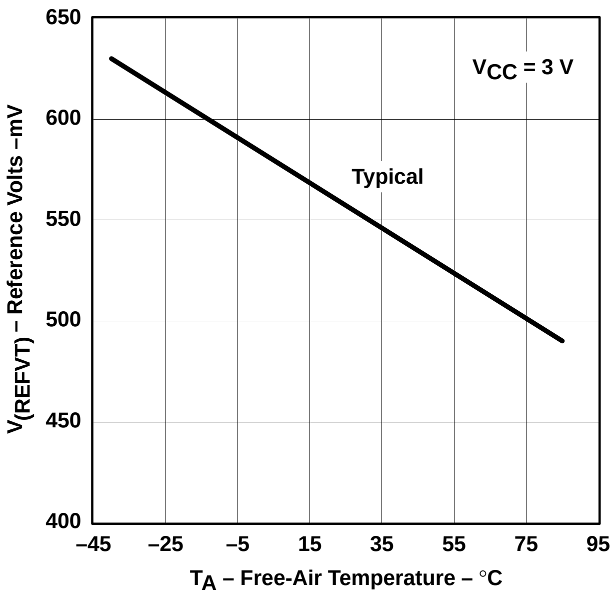


Figure 6. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

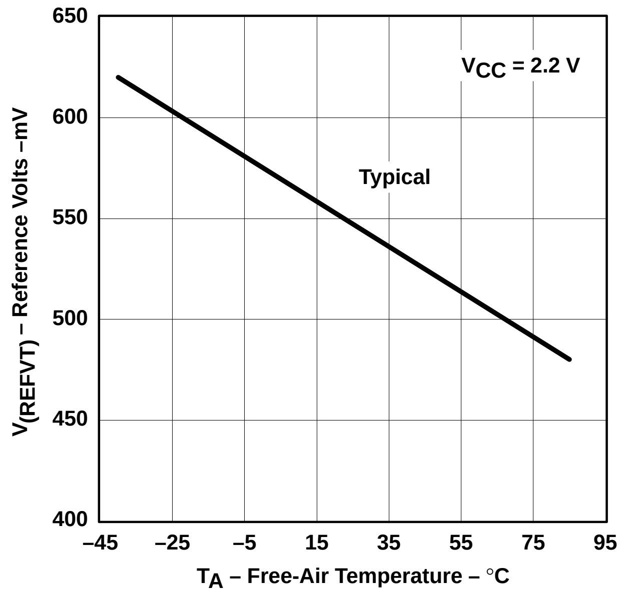


Figure 7. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

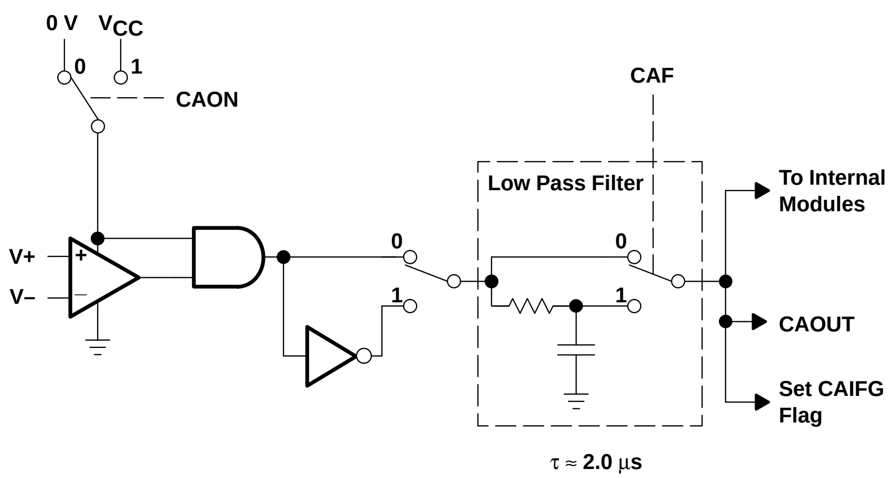


Figure 8. Block Diagram of Comparator_A Module

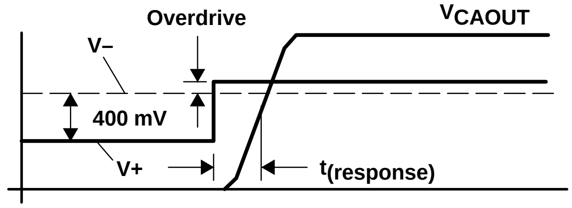


Figure 9. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

POR

PARAMETER		CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$t_{(POR\_Delay)}$	POR		2.2 V/3 V		150	250	µs
V_{POR}	POR	T_A = –40°C		1.4		1.8	V
		T_A = +25°C		1.1		1.5	V
		T_A = +85°C		0.8		1.2	V
$V_{(min)}$	POR			0		0.4	V
$t_{(Reset)}$	PUC/POR	Reset is accepted internally	2.2 V/3 V	2			µs

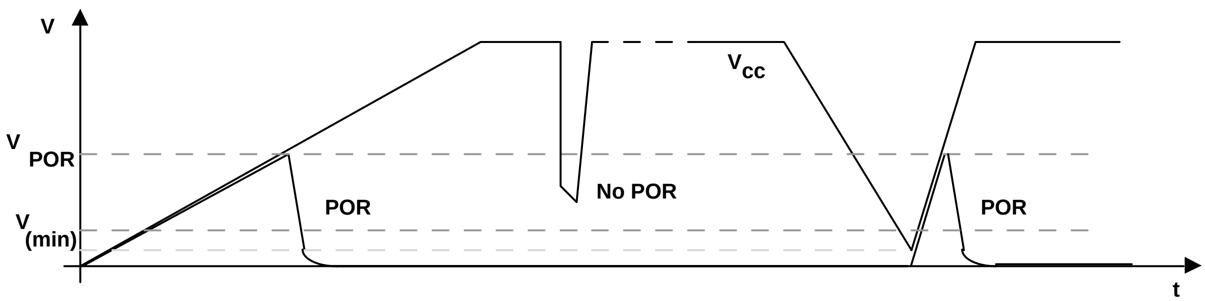


Figure 10. Power-On Reset (POR) vs Supply Voltage

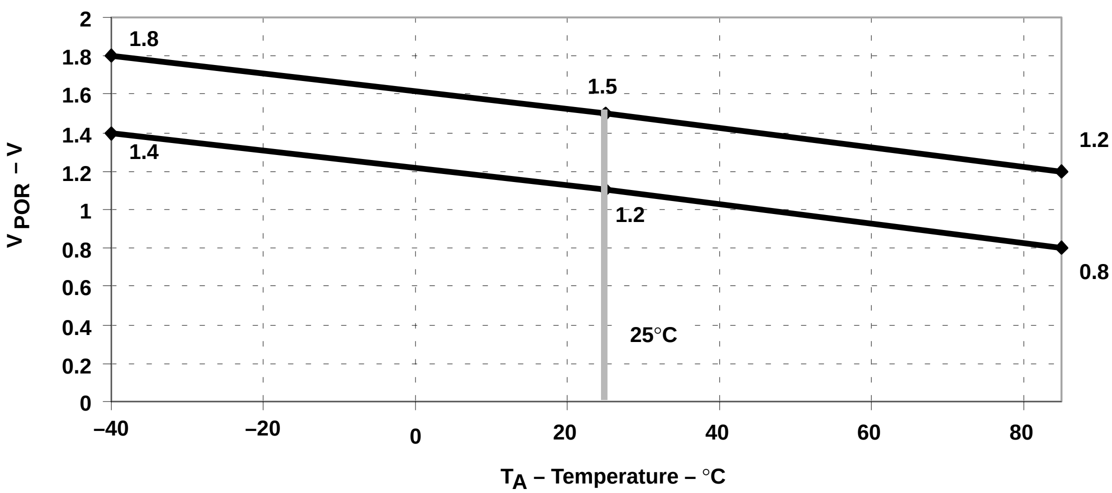


Figure 11. V_{POR} vs Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

DCO (see Note 1)

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(DCO03)}$	R_{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.08	0.12	0.15	MHz
		V_{CC} = 3 V	0.08	0.13	0.16	
$f_{(DCO13)}$	R_{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.14	0.19	0.23	MHz
		V_{CC} = 3 V	0.14	0.18	0.22	
$f_{(DCO23)}$	R_{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.22	0.30	0.36	MHz
		V_{CC} = 3 V	0.22	0.28	0.34	
$f_{(DCO33)}$	R_{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.37	0.49	0.59	MHz
		V_{CC} = 3 V	0.37	0.47	0.56	
$f_{(DCO43)}$	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.61	0.77	0.93	MHz
		V_{CC} = 3 V	0.61	0.75	0.90	
$f_{(DCO53)}$	R_{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1	1.2	1.5	MHz
		V_{CC} = 3 V	1	1.3	1.5	
$f_{(DCO63)}$	R_{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1.6	1.9	2.2	MHz
		V_{CC} = 3 V	1.69	2.0	2.29	
$f_{(DCO73)}$	R_{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	2.4	2.9	3.4	MHz
		V_{CC} = 3 V	2.7	3.2	3.65	
$f_{(DCO47)}$	R_{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V/3 V	$f_{DCO40} \times 1.7$	$f_{DCO40} \times 2.1$	$f_{DCO40} \times 2.5$	MHz
$f_{(DCO77)}$	R_{sel} = 7, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	4	4.5	4.9	MHz
		V_{CC} = 3 V	4.4	4.9	5.4	
$S_{(Rsel)}$	$S_R = f_{Rsel+1} / f_{Rsel}$	V_{CC} = 2.2 V/3 V	1.35	1.65	2	
$S_{(DCO)}$	$S_{DCO} = f_{DCO+1} / f_{DCO}$	V_{CC} = 2.2 V/3 V	1.07	1.12	1.16	
D_t	Temperature drift, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 2)	V_{CC} = 2.2 V	–0.31	–0.36	–0.40	%/°C
		V_{CC} = 3 V	–0.33	–0.38	–0.43	
D_V	Drift with V_{CC} variation, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 2)	V_{CC} = 2.2 V/3 V	0	5	10	%/V

NOTES: 1. The DCO frequency may not exceed the maximum system frequency defined by parameter processor frequency, $f_{(System)}$.
2. This parameter is not production tested.

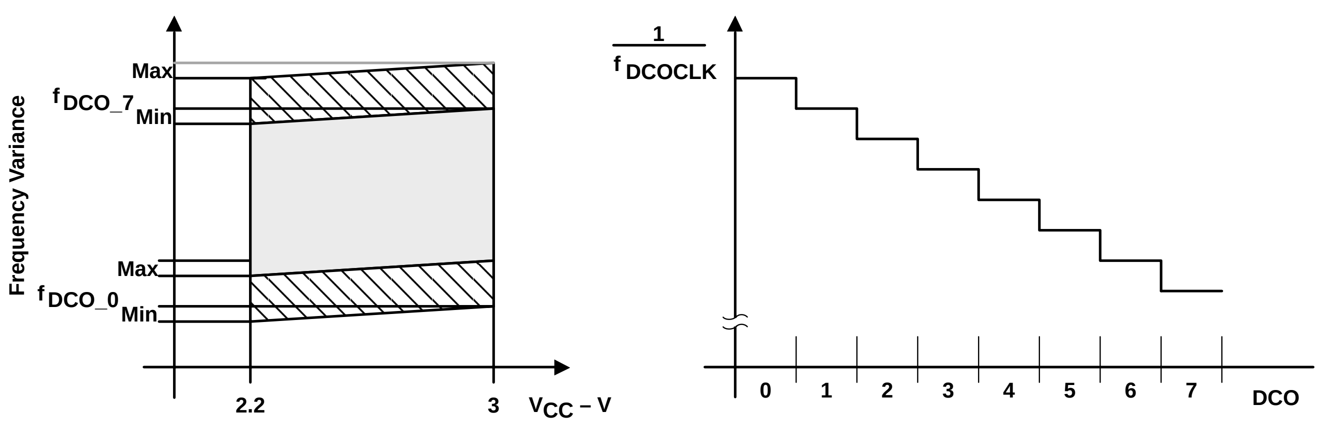


Figure 12. DCO Characteristics

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- Individual devices have a minimum and maximum operation frequency. The specified parameters for f_{DCOx0} to f_{DCOx7} are valid for all devices.
- All ranges selected by Rsel(n) overlap with Rsel(n+1): Rsel0 overlaps with Rsel1, ... Rsel6 overlaps with Rsel7.
- DCO control bits DCO0, DCO1, and DCO2 have a step size as defined by parameter S_{DCO}.
- Modulation control bits MOD0 to MOD4 select how often f_{DCO+1} is used within the period of 32 DCOCLK cycles. The frequency $f_{(DCO)}$ is used for the remaining cycles. The frequency is an average equal to $f(DCO) \times (2^{MOD/32})$.

crystal oscillator, LFXT1 oscillator (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
X_{CIN}	Integrated input capacitance	XTS=0; LF oscillator selected V_{CC} = 2.2 V/3 V		12		pF
		XTS=1; XT1 oscillator selected V_{CC} = 2.2 V/3 V		2		
X_{COUT}	Integrated output capacitance	XTS=0; LF oscillator selected V_{CC} = 2.2 V/3 V		12		pF
		XTS=1; XT1 oscillator selected V_{CC} = 2.2 V/3 V		2		
X_{INL}	Input levels at XIN, XOUT	V_{CC} = 2.2 V/3 V	V_{SS}		$0.2 \times V_{CC}$	V
X_{INH}		V_{CC} = 2.2 V/3 V	$0.8 \times V_{CC}$		V_{CC}	V

NOTE 1: The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.

crystal oscillator, XT2 oscillator (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
X_{CIN}	Integrated input capacitance	V_{CC} = 2.2 V/3 V		2		pF
X_{COUT}	Integrated output capacitance	V_{CC} = 2.2 V/3 V		2		pF
X_{INL}	Input levels at XIN, XOUT	V_{CC} = 2.2 V/3 V	V_{SS}		$0.2 \times V_{CC}$	V
X_{INH}		V_{CC} = 2.2 V/3 V	$0.8 \times V_{CC}$		V_{CC}	V

NOTE 1: The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.

USART0 (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(\tau)}$	USART0: deglitch time	V_{CC} = 2.2 V	200	430	800	ns
		V_{CC} = 3 V	150	280	500	

NOTE 1: The signal applied to the USART0 receive signal/terminal (URXD0) should meet the timing requirements of $t_{(t)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(t)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0 line.

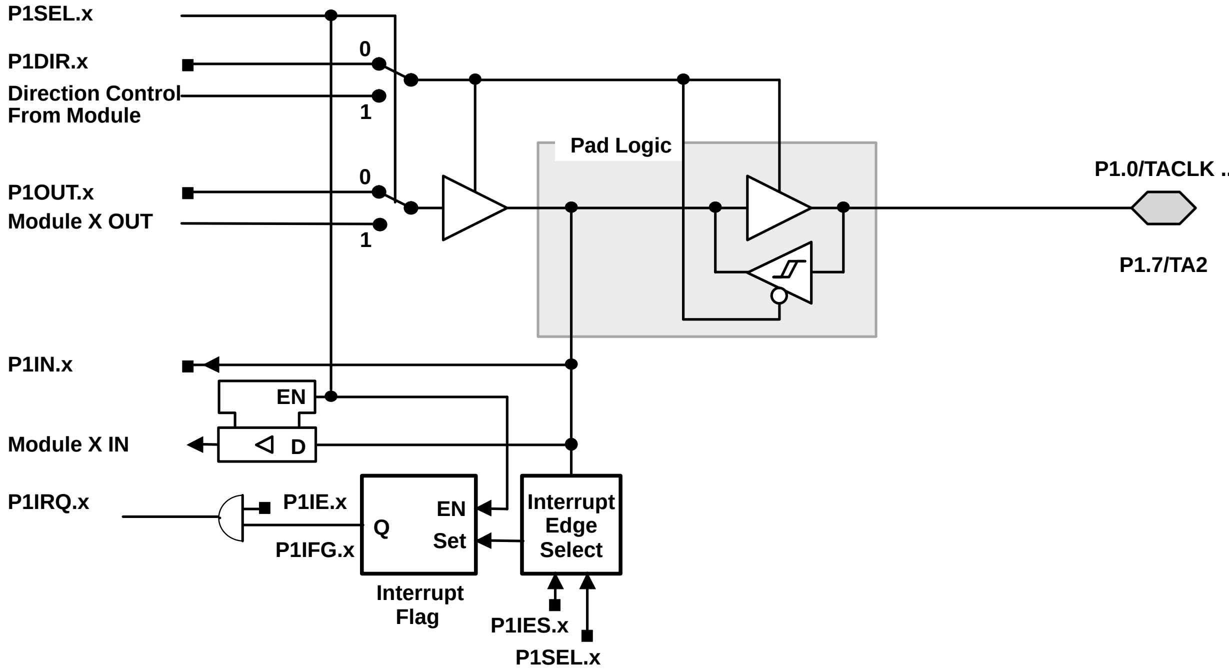
JTAG, fuse

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$f_{(TCK)}$	JTAG/test	TCK frequency	2.2 V	DC		5	MHz
			3 V	DC		10	
		Pullup resistors on TMS, TCK, TDI (see Note 1)	2.2 V/ 3V	25	60	90	kΩ
V_{FB}	JTAG/fuse (see Note 2)	Fuse-blow voltage (see Note 3)	3.6	5		5.5	V
I_{FB}		Supply current on TDI with fuse blown				100	mA
		Time to blow the fuse				20	ms

NOTES: 1. TMS, TDI, and TCK pull-up resistors are implemented in all F versions.
2. Once the fuse is blown, no further access to the MSP430 JTAG/test feature is possible. The JTAG block is switched to bypass mode.
3. The supply voltage to blow the fuse is applied to the TDI pin.

input/output schematic

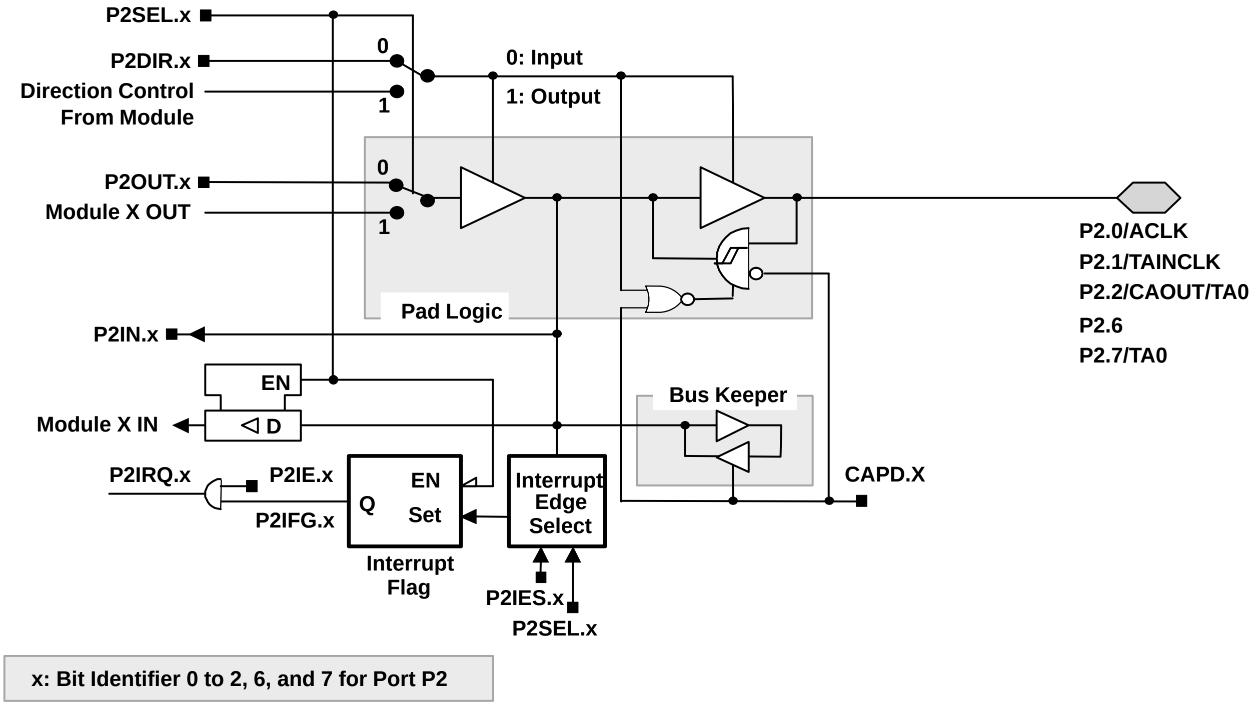
port P1, P1.0 to P1.7, input/output with Schmitt-trigger



PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	DV_{SS}	P1IN.0	TACLK†	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	Out0 signal†	P1IN.1	CCI0A†	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 signal†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	Out2 signal†	P1IN.3	CCI2A†	P1IE.3	P1IFG.3	P1IES.3
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	Out0 signal†	P1IN.5	unused	P1IE.5	P1IFG.5	P1IES.5
P1Sel.6	P1DIR.6	P1DIR.6	P1OUT.6	Out1 signal†	P1IN.6	unused	P1IE.6	P1IFG.6	P1IES.6
P1Sel.7	P1DIR.7	P1DIR.7	P1OUT.7	Out2 signal†	P1IN.7	unused	P1IE.7	P1IFG.7	P1IES.7

† Signal from or to Timer_A

port P2, P2.0 to P2.2, P2.6, and P2.7 input/output with Schmitt-trigger

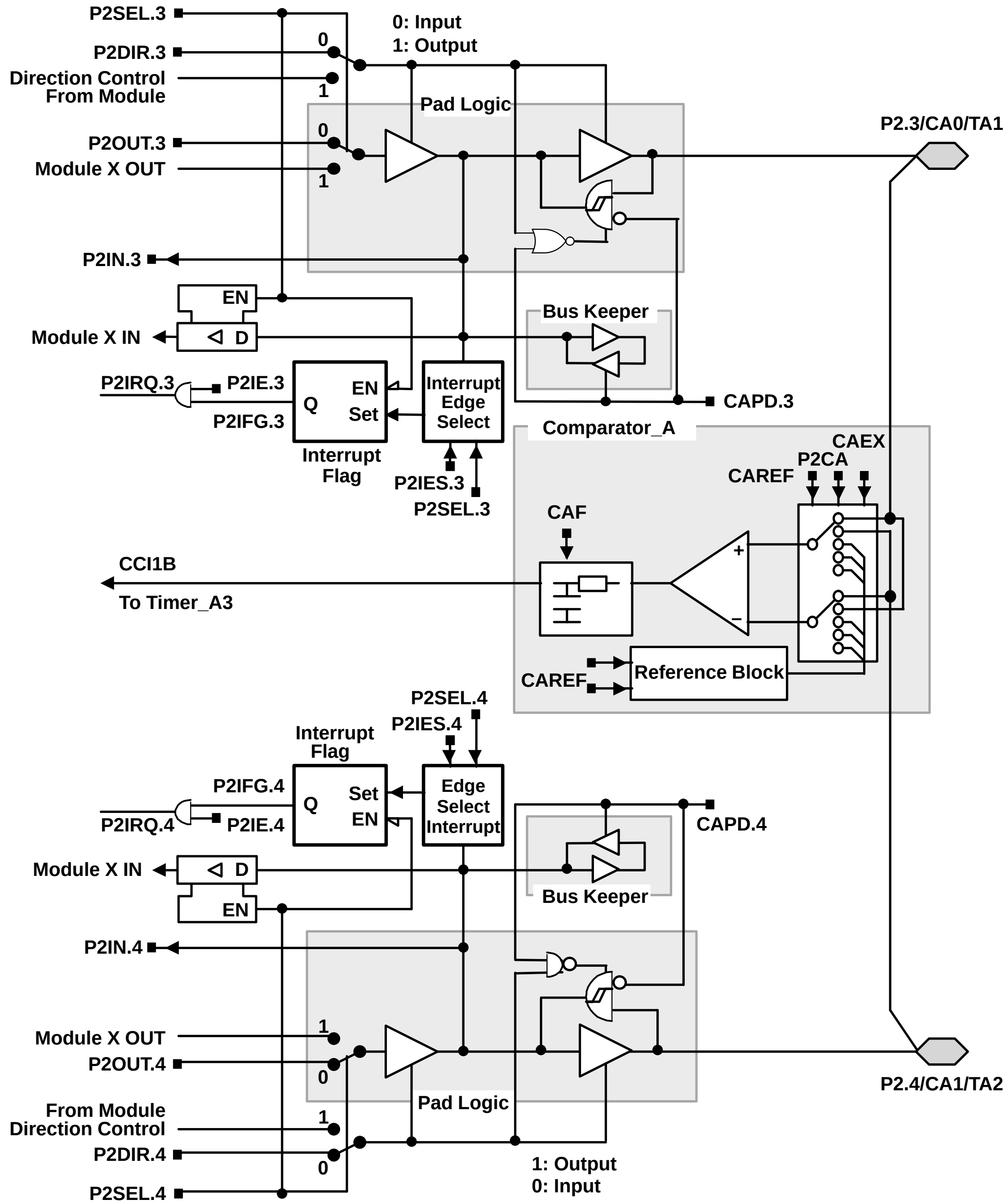


PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	ACLK	P2IN.0	unused	P2IE.0	P2IFG.0	P2IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	DV_{SS}	P2IN.1	INCLK‡	P2IE.1	P2IFG.1	P2IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	CAOUT†	P2IN.2	CCI0B‡	P2IE.2	P2IFG.2	P2IES.2
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	DV_{SS}	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	Out0 signal§	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

† Signal from Comparator_A
‡ Signal to Timer_A
§ Signal from Timer_A

input/output schematic (continued)

port P2, P2.3 to P2.4, input/output with Schmitt-trigger

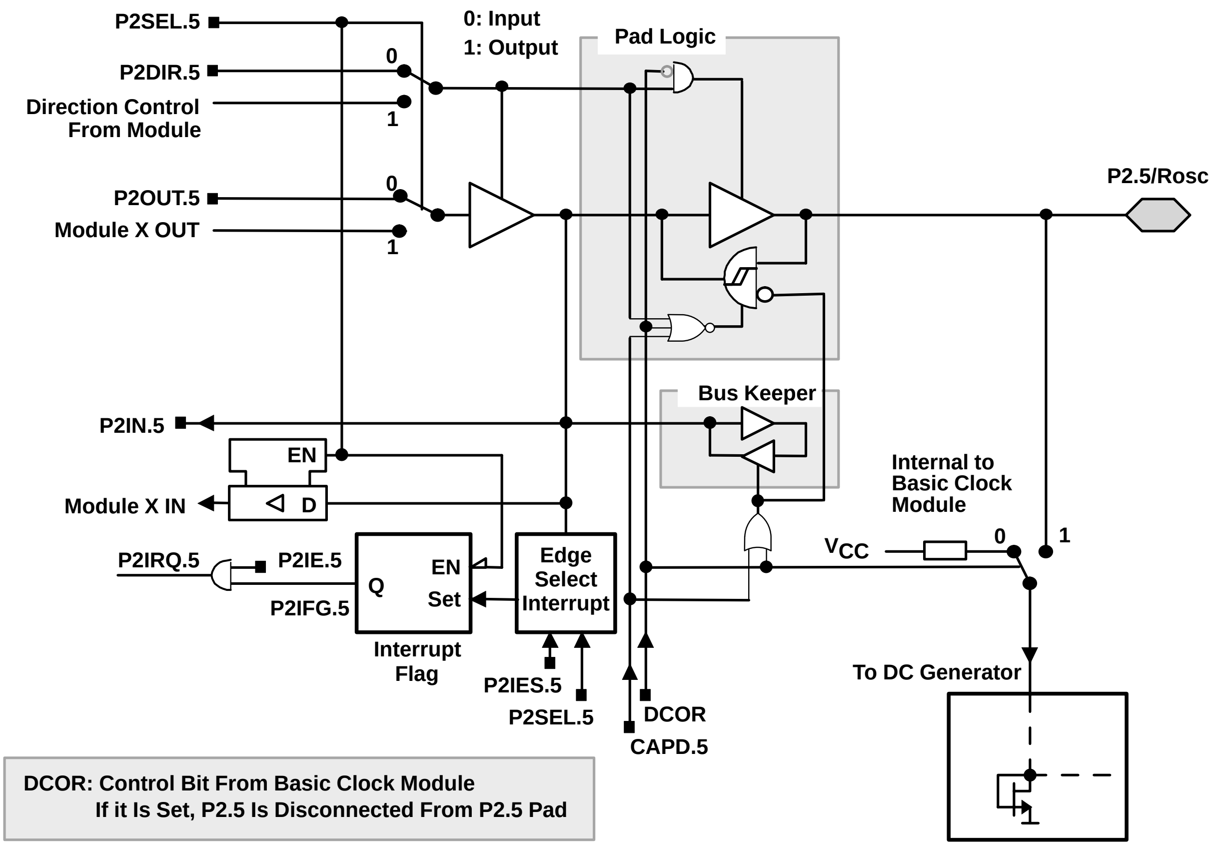


PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out1 signal†	P2IN.3	unused	P2IE.3	P2IFG.3	P2IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	Out2 signal†	P2IN.4	unused	P2IE.4	P2IFG.4	P2IES.4

† Signal from Timer_A

input/output schematic (continued)

port P2, P2.5, input/output with Schmitt-trigger and R_{OSC} function for the basic clock module

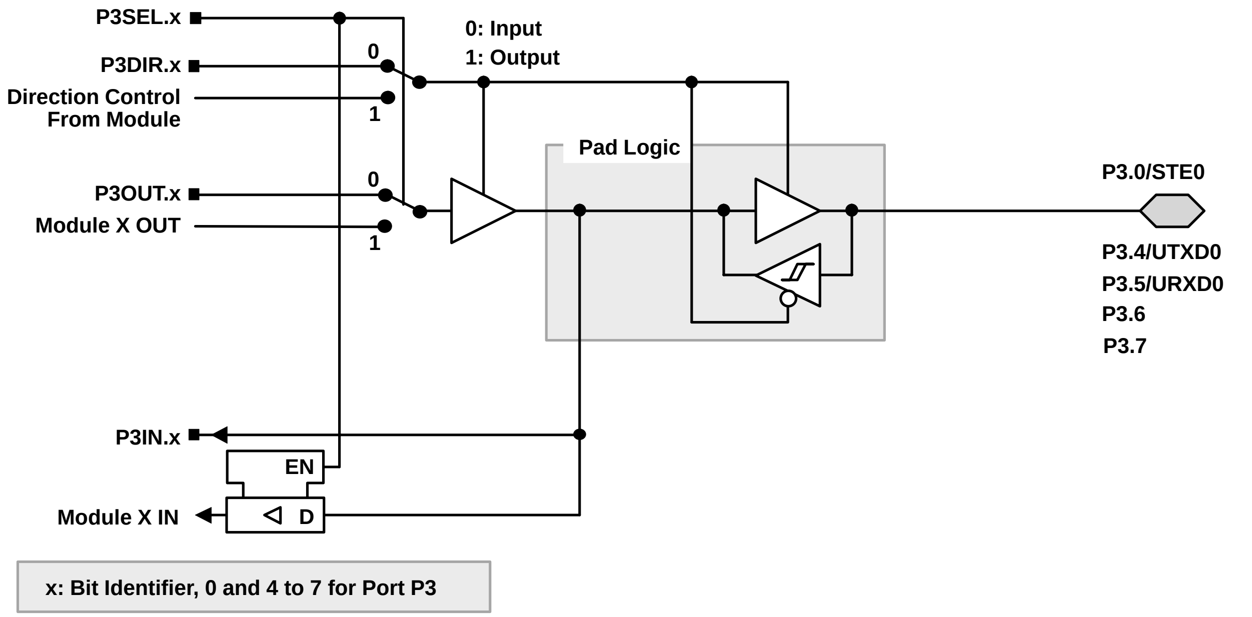


DCOR: Control Bit From Basic Clock Module
If it Is Set, P2.5 Is Disconnected From P2.5 Pad

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	DV_{SS}	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5

input/output schematic (continued)

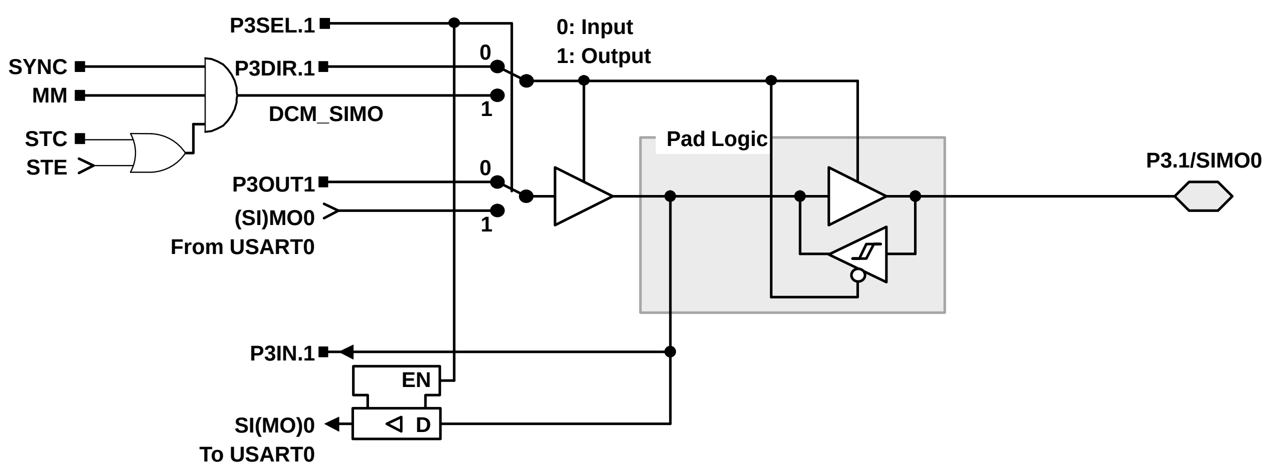
port P3, P3.0 and P3.4 to P3.7, input/output with Schmitt-trigger



PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P3Sel.0	P3DIR.0	DV_{SS}	P3OUT.0	DV_{SS}	P3IN.0	STE0
P3Sel.4	P3DIR.4	DV_{CC}	P3OUT.4	UTXD0†	P3IN.4	Unused
P3Sel.5	P3DIR.5	DV_{SS}	P3OUT.5	DV_{SS}	P3IN.5	URXD0‡
P3Sel.6	P3DIR.6	DV_{CC}	P3OUT.6	DV_{SS}	P3IN.6	Unused
P3Sel.7	P3DIR.7	DV_{SS}	P3OUT.7	DV_{SS}	P3IN.7	Unused

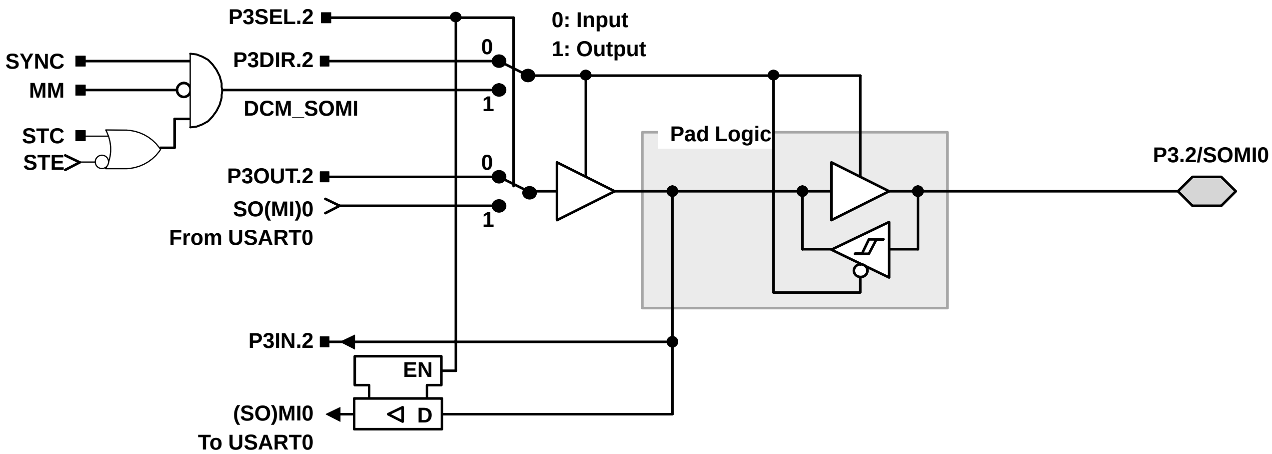
† Output from USART0 module
‡ Input to USART0 module

port P3, P3.1, input/output with Schmitt-trigger

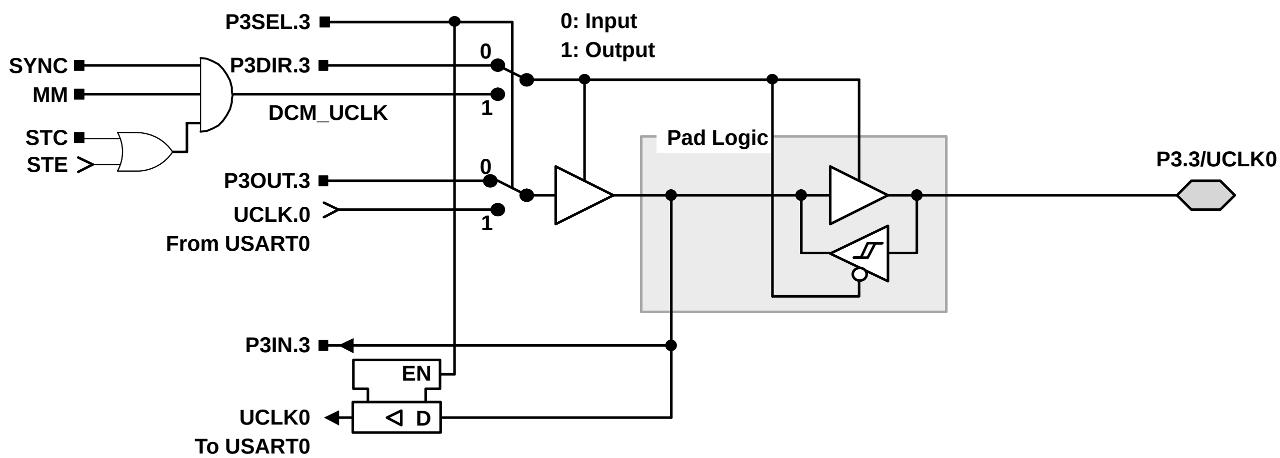


input/output schematic (continued)

port P3, P3.2, input/output with Schmitt-trigger



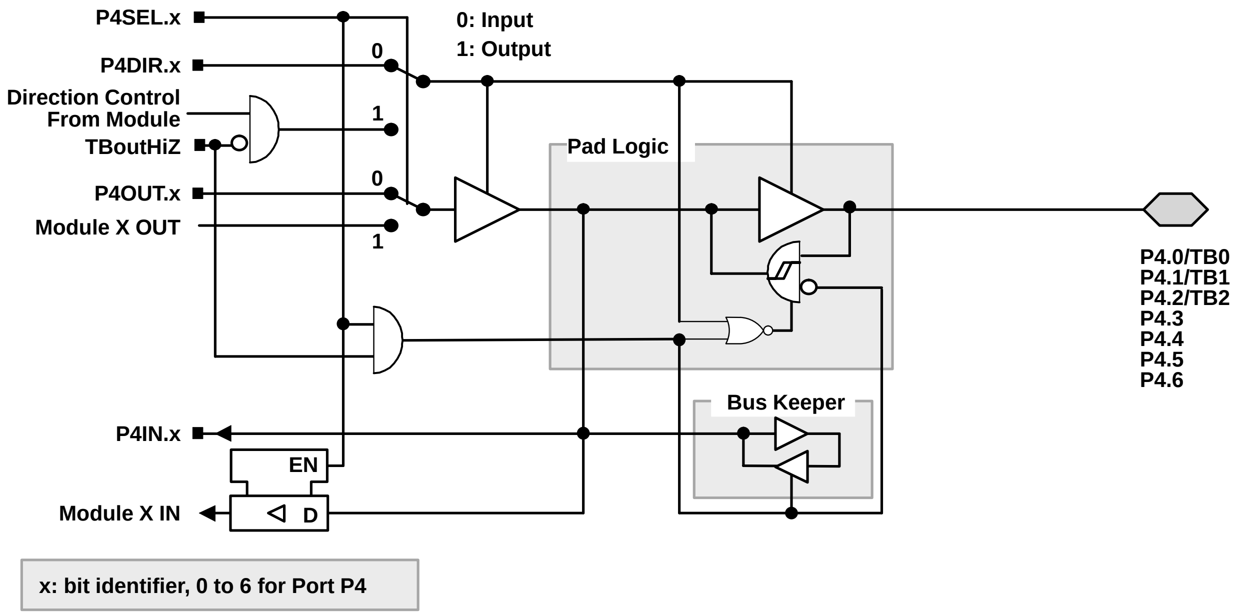
port P3, P3.3, input/output with Schmitt-trigger



NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, the P3.3/UCLK0 is always an input.
SPI, slave mode: The clock applied to UCLK0 is used to shift data in and out.
SPI, master mode: The clock to shift data in and out is supplied to connected devices on pin P3.3/UCLK0 (in slave mode).

input/output schematic (continued)

port P4, P4.0 to P4.6, input/output with Schmitt-trigger



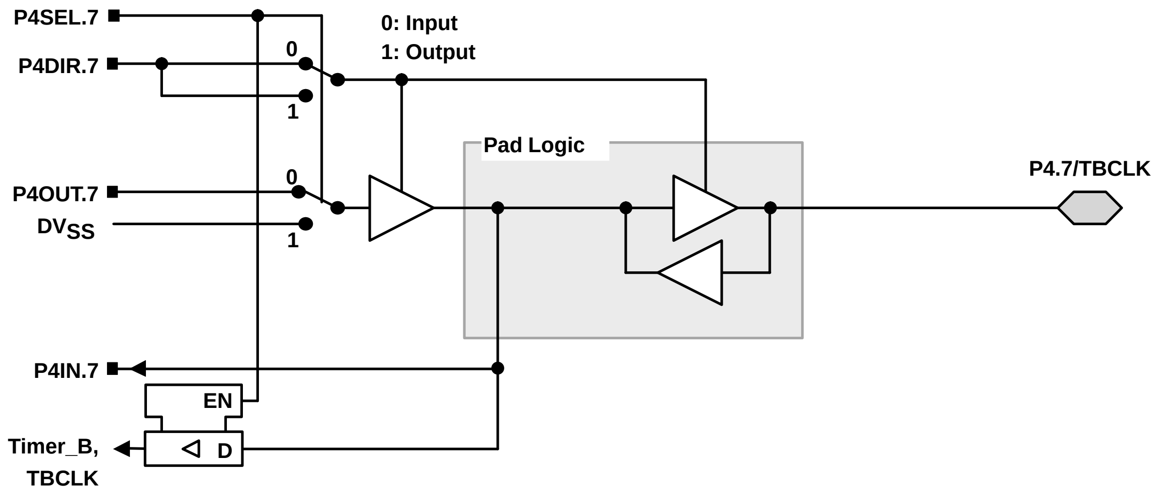
PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P4Sel.0	P4DIR.0	P4DIR.0	P4OUT.0	Out0 signal†	P4IN.0	CCI0A / CCI0B‡
P4Sel.1	P4DIR.1	P4DIR.1	P4OUT.1	Out1 signal†	P4IN.1	CCI1A / CCI1B‡
P4Sel.2	P4DIR.2	P4DIR.2	P4OUT.2	Out2 signal†	P4IN.2	CCI2A / CCI2B‡
P4Sel.3	P4DIR.3	P4DIR.3	P4OUT.3	DV_{SS}	P4IN.3	Unused
P4Sel.4	P4DIR.4	P4DIR.4	P4OUT.4	DV_{SS}	P4IN.4	Unused
P4Sel.5	P4DIR.5	P4DIR.5	P4OUT.5	DV_{SS}	P4IN.5	Unused
P4Sel.6	P4DIR.6	P4DIR.6	P4OUT.6	DV_{SS}	P4IN.6	Unused

† Signal from Timer_B
‡ Signal to Timer_B

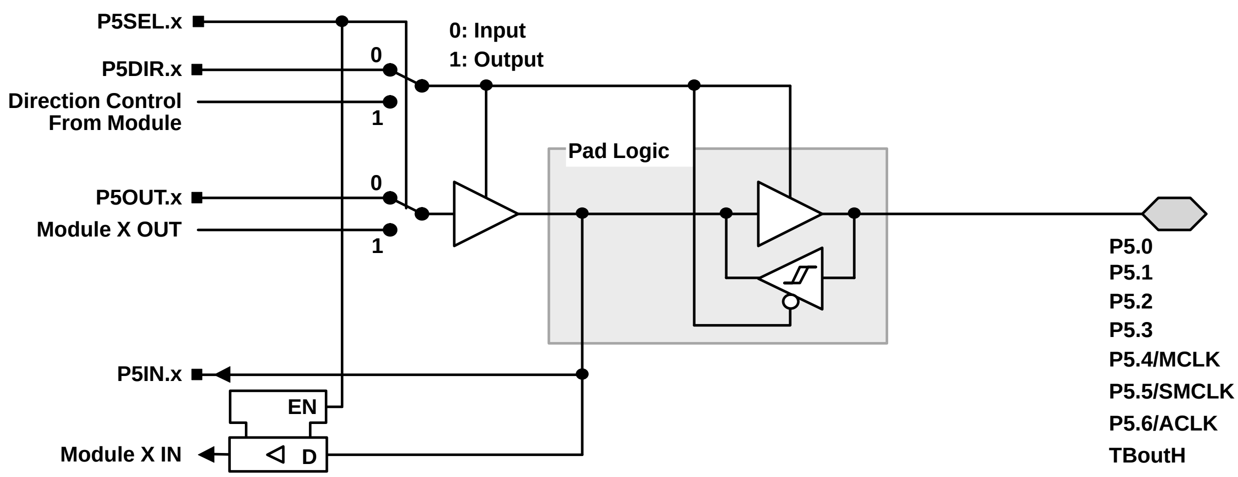
NOTE: TBoutHiZ signal is used by port module P4, pins P4.0 to P4.6. The function TBoutHiZ is mainly used with Timer_B. Port pins P4.3 to P4.6 have the TBoutHiZ function, but no Timer_B output is available for secondary functions. The port selection function can be used to get the port pin to high impedance and to use the P4DIR.x bits.

input/output schematic (continued)

port P4, P4.7, input/output with Schmitt-trigger



port P5, P5.0 to P5.7, input/output with Schmitt-trigger



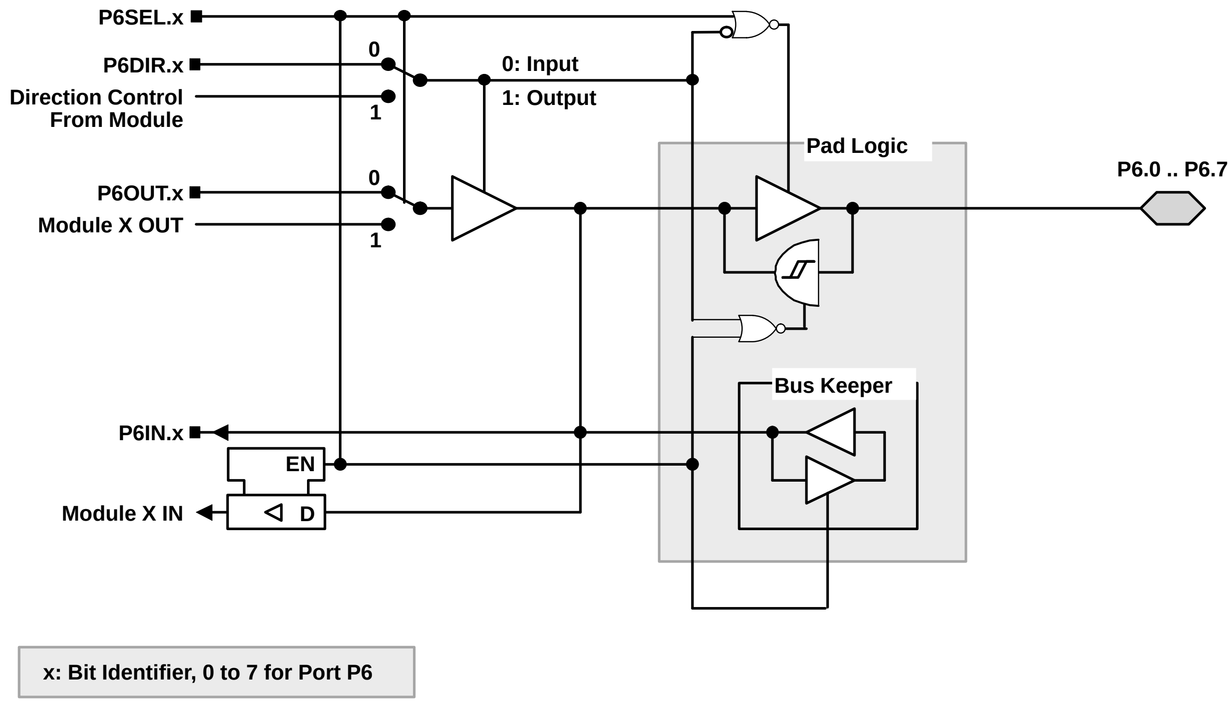
x: Bit Identifier, 0 to 7 for Port P5

PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P5Sel.0	P5DIR.0	DV_{SS}	P5OUT.0	DV_{SS}	P5IN.0	unused
P5Sel.1	P5DIR.1	DV_{CC}	P5OUT.1	DV_{SS}	P5IN.1	unused
P5Sel.2	P5DIR.2	DV_{CC}	P5OUT.2	DV_{SS}	P5IN.2	unused
P5Sel.3	P5DIR.3	DV_{CC}	P5OUT.3	DV_{SS}	P5IN.3	unused
P5Sel.4	P5DIR.4	DV_{CC}	P5OUT.4	MCLK	P5IN.4	unused
P5Sel.5	P5DIR.5	DV_{CC}	P5OUT.5	SMCLK	P5IN.5	unused
P5Sel.6	P5DIR.6	DV_{CC}	P5OUT.6	ACLK	P5IN.6	unused
P5Sel.7	P5DIR.7	DV_{SS}	P5OUT.7	DV_{SS}	P5IN.7	TBoutHiZ

NOTE: TBoutHiZ signal is used by port module P4, pins P4.0 to P4.6. The function of TBoutHiZ is mainly useful when used with Timer_B.

input/output schematic (continued)

port P6, P6.0 to P6.7, input/output with Schmitt-trigger

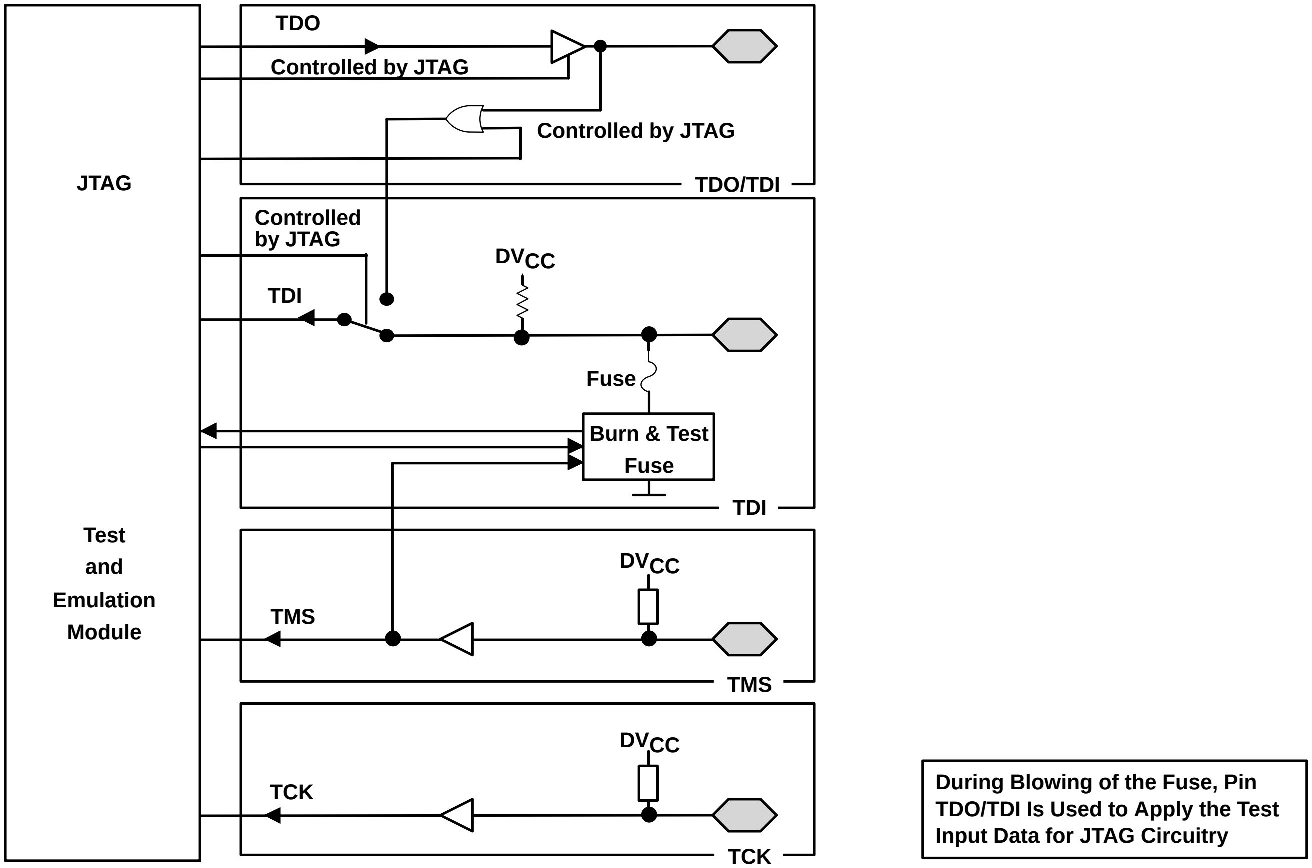


PnSel.x	PnDIR.x	DIR. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P6Sel.0	P6DIR.0	P6DIR.0	P6OUT.0	DV_{SS}	P6IN.0	unused
P6Sel.1	P6DIR.1	P6DIR.1	P6OUT.1	DV_{SS}	P6IN.1	unused
P6Sel.2	P6DIR.2	P6DIR.2	P6OUT.2	DV_{SS}	P6IN.2	unused
P6Sel.3	P6DIR.3	P6DIR.3	P6OUT.3	DV_{SS}	P6IN.3	unused
P6Sel.4	P6DIR.4	P6DIR.4	P6OUT.4	DV_{SS}	P6IN.4	unused
P6Sel.5	P6DIR.5	P6DIR.5	P6OUT.5	DV_{SS}	P6IN.5	unused
P6Sel.6	P6DIR.6	P6DIR.6	P6OUT.6	DV_{SS}	P6IN.6	unused
P6Sel.7	P6DIR.7	P6DIR.7	P6OUT.7	DV_{SS}	P6IN.7	unused

NOTE: Direction control bits P6DIR.x and P6SEL.x control whether the port function is active (P6DIR.x=0) or whether the input P6.x is in the high-impedance state. This is identical to the port P6 function in the MSP430F13x devices (used for emulation/prototyping), but different from other digital-only ports such as P5.

input/output schematic (continued)

JTAG pins TMS, TCK, TDI, TDO/TDI, input/output with Schmitt-trigger



JTAG fuse check mode

MSP430 devices that have the fuse on the TDI terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1 mA at 3 V can flow from the TDI pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 15). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

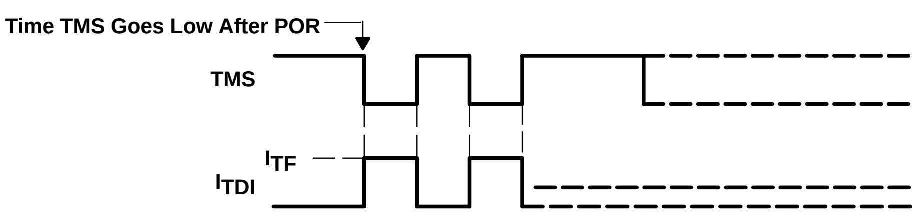
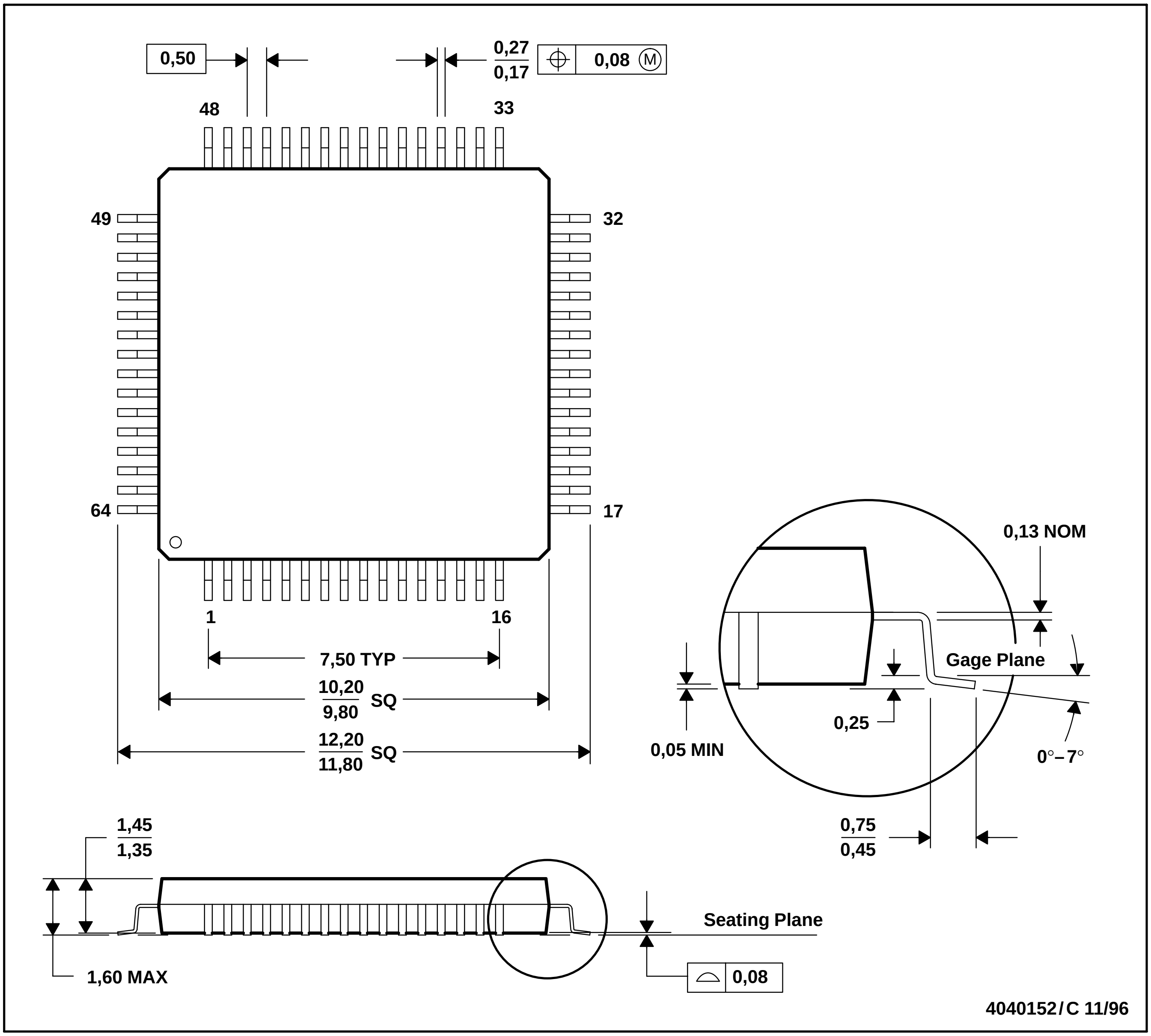


Figure 13. Fuse Check Mode Current

MECHANICAL DATA

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

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