

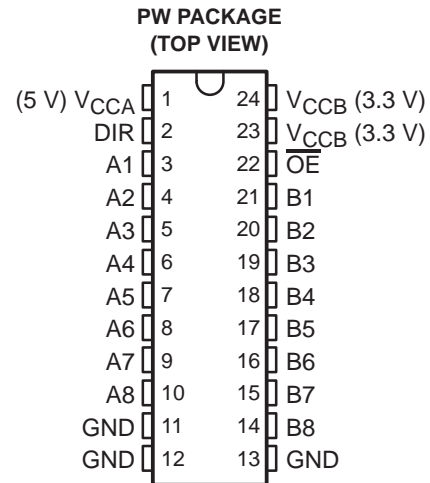
# SN74LVC4245A-EP

## OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

SCAS742 – DECEMBER 2003

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Bidirectional Voltage Translator**
- **5.5 V on A Port and 2.7 V to 3.6 V on B Port**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



### description/ordering information

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has  $V_{CCB}$ , which is set at 3.3 V, and A port has  $V_{CCA}$ , which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa.

The SN74LVC4245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

The SN74LVC4245A pinout allows the designer to switch to a normal all-3.3-V or all-5-V 20-pin '245 device without board re-layout. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245A to align with the conventional '245 pinout.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PW   Reel of 2000	SN74LVC4245AIPWREP	C4245AEP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



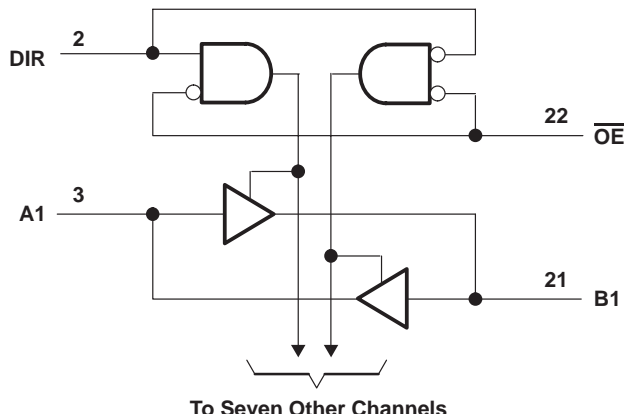
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated

# SN74LVC4245A-EP OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

SCAS742 – DECEMBER 2003

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range for $V_{CCA} = 4.5\text{ V to }5.5\text{ V}$ (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CCA}$ .....	-0.5 V to 6.5 V
Input voltage range, $V_I$ : A port (see Note 1) .....	-0.5 V to $V_{CCA} + 0.5\text{ V}$
Control inputs .....	-0.5 V to 6 V
Output voltage range, $V_O$ : A port (see Note 1) .....	-0.5 V to $V_{CCA} + 0.5\text{ V}$
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ .....	$\pm 50\text{ mA}$
Continuous current through each $V_{CCA}$ or GND .....	$\pm 100\text{ mA}$
Package thermal impedance, $\theta_{JA}$ (see Note 2) .....	88°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. This value is limited to 6 V maximum.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## absolute maximum ratings over operating free-air temperature range for $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$ (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CCB}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ : B port (see Note 3) .....	-0.5 V to $V_{CCB} + 0.5\text{ V}$
Output voltage range, $V_O$ : B port (see Note 3) .....	-0.5 V to $V_{CCB} + 0.5\text{ V}$
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ .....	$\pm 50\text{ mA}$
Continuous current through $V_{CCB}$ or GND .....	$\pm 100\text{ mA}$
Package thermal impedance, $\theta_{JA}$ (see Note 2) .....	88°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 2. The package thermal impedance is calculated in accordance with JESD 51-7.  
3. This value is limited to 4.6 V maximum.



**SN74LVC4245A-EP**  
**OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER**  
**WITH 3-STATE OUTPUTS**

SCAS742 – DECEMBER 2003

**recommended operating conditions for  $V_{CCA} = 4.5\text{ V to }5.5\text{ V}$  (see Note 4)**

		MIN	MAX	UNIT
$V_{CCA}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CCA}$	V
$V_O$	Output voltage	0	$V_{CCA}$	V
$I_{OH}$	High-level output current		-24	mA
$I_{OL}$	Low-level output current		24	mA
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 4: All unused inputs of the device must be held at the associated  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**recommended operating conditions for  $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$  (see Note 4)**

			MIN	MAX	UNIT
$V_{CCB}$	Supply voltage		2.7	3.6	V
$V_{IH}$	High-level input voltage	$V_{CCB} = 2.7\text{ V to }3.6\text{ V}$	2		V
$V_{IL}$	Low-level input voltage	$V_{CCB} = 2.7\text{ V to }3.6\text{ V}$		0.8	V
$V_I$	Input voltage		0	$V_{CCB}$	V
$V_O$	Output voltage		0	$V_{CCB}$	V
$I_{OH}$	High-level output current	$V_{CCB} = 2.7\text{ V}$		-12	mA
		$V_{CCB} = 3\text{ V}$		-24	
$I_{OL}$	Low-level output current	$V_{CCB} = 2.7\text{ V}$		12	mA
		$V_{CCB} = 3\text{ V}$		24	
$T_A$	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at the associated  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74LVC4245A-EP

## OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER

### WITH 3-STATE OUTPUTS

SCAS742 – DECEMBER 2003

electrical characteristics over recommended operating free-air temperature range for  $V_{CCA} = 4.5\text{ V to }5.5\text{ V}$  (unless otherwise noted) (see Note 5)

PARAMETER		TEST CONDITIONS	$V_{CCA}$	MIN	TYP†	MAX	UNIT
$V_{OH}$		$I_{OH} = -100\ \mu\text{A}$	4.5 V	4.3		V	
			5.5 V	5.3			
		$I_{OH} = -24\ \text{mA}$	4.5 V	3.7			
			5.5 V	4.7			
$V_{OL}$		$I_{OL} = 100\ \mu\text{A}$	4.5 V	0.2		V	
			5.5 V	0.2			
		$I_{OL} = 24\ \text{mA}$	4.5 V	0.55			
			5.5 V	0.55			
$I_I$	Control inputs	$V_I = V_{CCA}$ or GND	5.5 V			$\pm 1$	$\mu\text{A}$
$I_{OZ}^\ddagger$	A port	$V_O = V_{CCA}$ or GND	5.5 V			$\pm 5$	$\mu\text{A}$
$I_{CCA}$		$V_I = V_{CCA}$ or GND, $I_O = 0$	5.5 V			80	$\mu\text{A}$
$\Delta I_{CCA}^\S$		One input at 3.4 V, Other inputs at $V_{CCA}$ or GND	5.5 V			1.5	mA
$C_i$	Control inputs	$V_I = V_{CCA}$ or GND	Open	5			pF
$C_{io}$	A port	$V_O = V_{CCA}$ or GND	5 V	11			pF

† All typical values are measured at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated  $V_{CC}$ .

NOTE 5:  $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$

electrical characteristics over recommended operating free-air temperature range for  $V_{CCB} = 2.7\text{ V to }3.6\text{ V}$  (unless otherwise noted) (see Note 6)

PARAMETER		TEST CONDITIONS	$V_{CCB}$	MIN	TYP†	MAX	UNIT
$V_{OH}$		$I_{OH} = -100\ \mu\text{A}$	2.7 V to 3.6 V	$V_{CC} - 0.2$		V	
			2.7 V	2.2			
		$I_{OH} = -12\ \text{mA}$	3 V	2.4			
			3 V	2			
$V_{OL}$		$I_{OL} = 100\ \mu\text{A}$	2.7 V to 3.6 V	0.2		V	
			2.7 V	0.4			
		$I_{OL} = 24\ \text{mA}$	3 V	0.55			
$I_{OZ}^\ddagger$	B port	$V_O = V_{CCB}$ or GND	3.6 V			$\pm 5$	$\mu\text{A}$
$I_{CCB}$		$V_I = V_{CCB}$ or GND, $I_O = 0$	3.6 V			50	$\mu\text{A}$
$\Delta I_{CCB}^\S$		One input at $V_{CCB} - 0.6\text{ V}$ , Other inputs at $V_{CCB}$ or GND	2.7 V to 3.6 V			0.5	mA
$C_{io}$	B port	$V_O = V_{CCB}$ or GND	3.3 V	11			pF

‡ For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated  $V_{CC}$ .

† All typical values are measured at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

NOTE 6:  $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$



# SN74LVC4245A-EP OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

SCAS742 – DECEMBER 2003

switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA} = 5 V \pm 0.5 V$ , $V_{CCB} = 2.7 V$ TO $3.6 V$		UNIT
			MIN	MAX	
$t_{PHL}$	A	B	1	6.3	ns
$t_{PLH}$			1	6.7	
$t_{PHL}$	B	A	1	6.1	ns
$t_{PLH}$			1	5	
$t_{PZL}$	$\overline{OE}$	A	1	9	ns
$t_{PZH}$			1	8.1	
$t_{PZL}$	$\overline{OE}$	B	1	8.8	ns
$t_{PZH}$			1	9.8	
$t_{PLZ}$	$\overline{OE}$	A	1	7	ns
$t_{PHZ}$			1	5.8	
$t_{PLZ}$	$\overline{OE}$	B	1	7.7	ns
$t_{PHZ}$			1	7.8	

operating characteristics,  $V_{CCA} = 4.5 V$  to  $5.5 V$ ,  $V_{CCB} = 2.7 V$  to  $3.6 V$ ,  $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per transceiver	$C_L = 0$ , $f = 10$ MHz	39.5	pF
			5	

## power-up considerations†

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems.

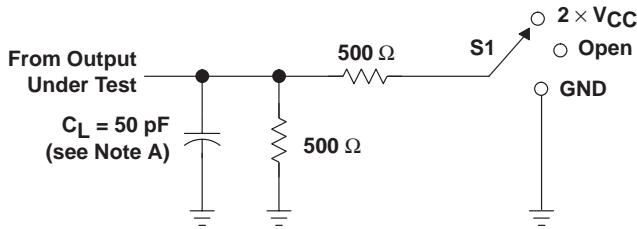
1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device ( $V_{CCA}$  for all four of these devices).
3. Tie  $\overline{OE}$  to  $V_{CCA}$  with a pullup resistor so that it ramps with  $V_{CCA}$ .
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with  $V_{CCA}$ . Otherwise, keep DIR low.

† Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

# SN74LVC4245A-EP OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

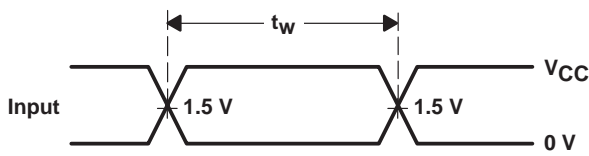
SCAS742 – DECEMBER 2003

## PARAMETER MEASUREMENT INFORMATION A PORT

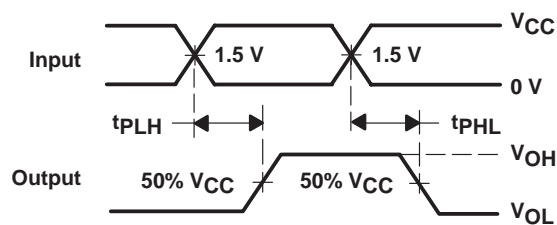


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

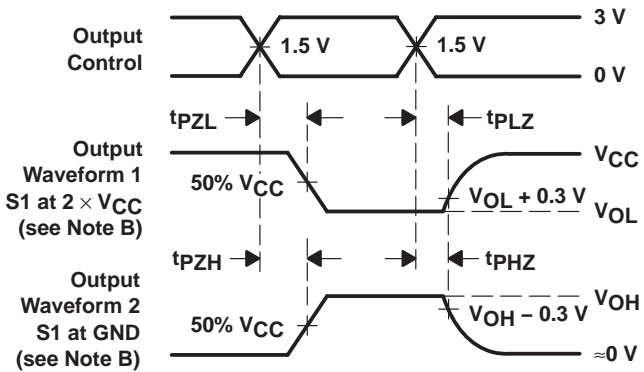
LOAD CIRCUIT



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
NONINVERTING OUTPUTS

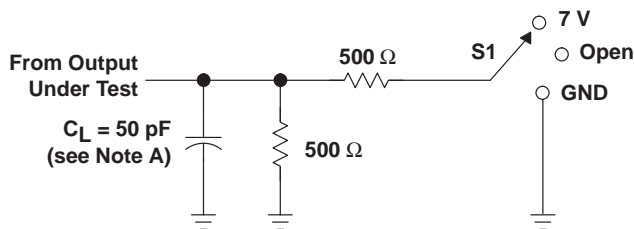


VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

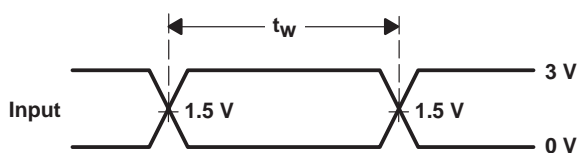
Figure 1. Load Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION**  
**B PORT**

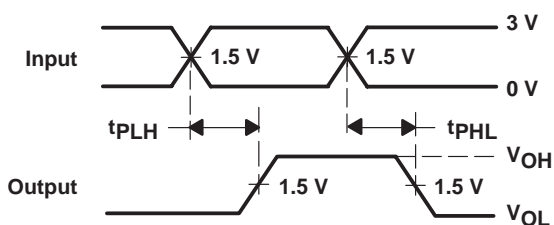


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	GND

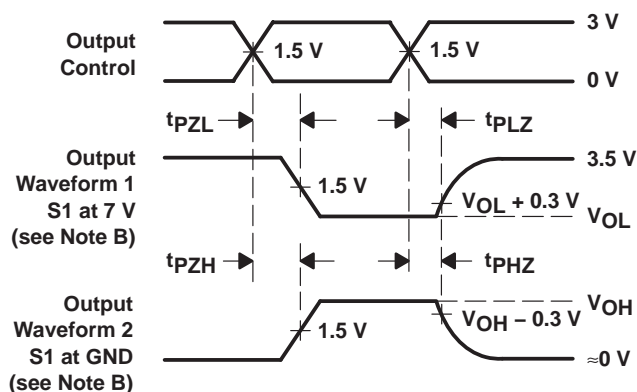
**LOAD CIRCUIT**



**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVC4245AIPWREP	ACTIVE	TSSOP	PW	24	2000	TBD	Call TI	Level-1-250C-UNLIM
V62/04664-01XE	ACTIVE	TSSOP	PW	24	2000	TBD	Call TI	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVC4245AIPWREP	ACTIVE	TSSOP	PW	24	2000	TBD	CU NIPDAU	Level-1-250C-UNLIM
V62/04664-01XE	ACTIVE	TSSOP	PW	24	2000	TBD	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVC4245AIPWREP	ACTIVE	TSSOP	PW	24	2000	TBD	Call TI	Level-1-250C-UNLIM
V62/04664-01XE	ACTIVE	TSSOP	PW	24	2000	TBD	Call TI	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265