

Ultralow-Power Supply Voltage Supervisor Family TPS383x

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ABSTRACT

Supply voltage supervisors have found their solid place in digital systems. They monitor the system's supply voltage and ensure a correct initialization of the circuits connected. The trend with digital integrated circuits with extremely low current consumption requires an equivalent reduction of the power dissipation of analog circuits. This report describes an advanced supply voltage supervisor circuit that distinguishes itself by an extremely low supply current, and therefore finds applications in battery-operated systems.

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1 Introduction

Continuous advances in semiconductor-technology have led to more efficient integrated circuits. This is combined with a constant reduction of the circuit's power dissipation, resulting in the design of equipment, that can be operated economically from a battery over a long period. In many cases, the designer only requests a function of the circuit if executing a current task, e.g. in a measurement recording system to sample and store a new date. Until a new measurement can be taken, a certain time elapses in which the circuit can fall into a sleeping mode. In this mode, only basic functions are active, e.g. the clock generator, while the remaining parts of the system are placed in a low-power idle state. This technique is allowed in systems where the average current consumption is in the range of few microamperes only. Such an application demands an extreme low-power dissipation of all integrated circuits in the system.

The supply voltage monitoring circuits that initialize the system also belong to the circuits. These devices must be constantly active and are therefore highly responsible for a considerable part of the supply current.

After turning on the supply voltage, the user must be aware of the defined initial state of all digital circuits. Starting from the initial state, a state machine steps sequentially from this state to the next. In a computer, the sequential operation of the program starts at a predefined program counter state. Logic circuits, like flip-flops, usually provide static set and reset inputs for this purpose. A high level or low level at these inputs forces the circuit into the desired state. Complex circuits like microprocessors or computers provide a reset input where an appropriate logic level at this input sets the circuit into a defined initial state. The data sheets of the circuits often show a circuit similar to Figure 1 to generate the reset signal when switching on the supply voltage.

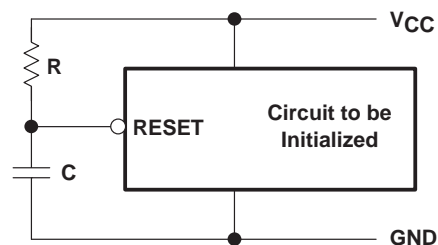


Figure 1. Simple Circuit to Produce a Reset Signal

An R/C-network at the reset input will delay the rise of the voltage at this point after switching on the supply-voltage. The desired reset signal is then generated. The dimensioning of the R/C network is not simple. The reset signal at this input must be held a certain time period, usually some microseconds, as long as a sequential micro-program in the processor has forced critical parts of the processor into a defined initial state. Also, the rise time of the supply voltage must be known in order to calculate the necessary time constant of the R/C-network. However, this is usually not the case, Therefore, additional measures are necessary, to assure the correct initialization of the system (see section 2.6).

With battery-operated systems, one must take into account the discharge characteristic of the battery in use (see Figure 2). Rechargeable batteries reach their full capacity if loaded up to the charge cut-off voltage. After completion of the charge process, the voltage sinks quickly to the open circuit voltage. The actual working range lies between the open circuit voltage and the end voltage. If the voltage of the battery becomes lower than the end voltage, the capacity of the battery is exhausted. The charge still remaining in the battery is not usable. Moreover, in the following time the user must take care that the battery is not discharged below the discharge cut-off voltage. Some rechargeable batteries become permanently damaged when discharged below this level.

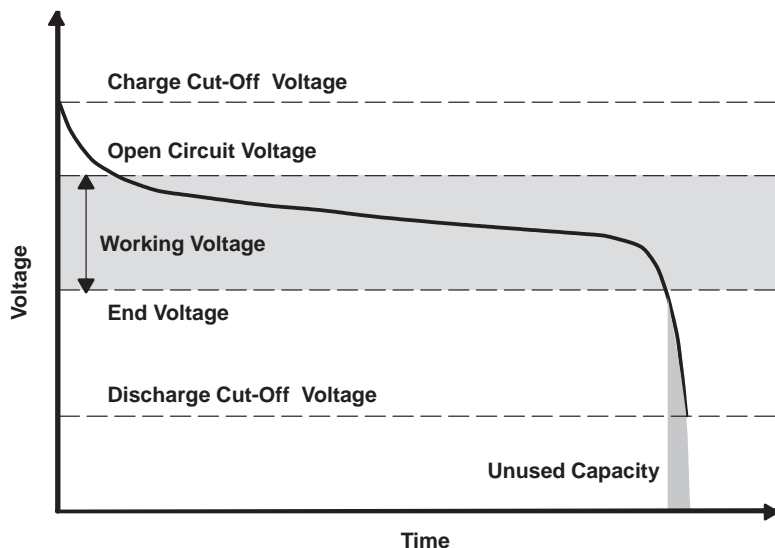


Figure 2. Discharge Characteristics of a Battery

Therefore, the task of the supply voltage supervisor not only includes controlling a defined initial state after switching on of the system's supply voltage, but also the circuit monitors the supply voltage during the entire operating time. At the end of the useful operating time, when the supply voltage drops below the end voltage, it generates a reset signal. Now its task is not to reinitialize the system but to force it into a defined idle state. If the supply voltage falls under the minimum level specified in the data sheet, the integrated circuits will not function properly. Therefore, unpredictable reactions of the system which may now occur must be prevented under all circumstances.

2 Circuit Description

2.1 Internal Operation of the Circuit

The basic item of the monitoring device (see Figure 3) forms the comparator that compares the voltage of a high-stable band-gap-reference with the supply voltage V_{DD} divided by the voltage divider $R1/R2$ and the capacitors $C1/C2$ connected in parallel to $R1/R2$. If the divided supply voltage is smaller than the reference voltage, the comparator's output becomes low and triggers the reset logic. The RESET output becomes high and the complementary $\overline{\text{RESET}}$ output goes low. If the supply voltage increases, so that the comparator output becomes high again, this positive edge triggers the timer in the reset logic. The timer holds the outputs further in the active state for the time t_d (see section 2.6).

In the same manner, a low level at the $\overline{\text{MR}}$ (manual reset) input activates the outputs of the device. This input is used to force the initialization of the circuit in Figure 3 by a logic signal. Users can also activate this process through a switch connected to this input. The resistor R3 provides a high level if the switch is open or if this input is left unconnected.

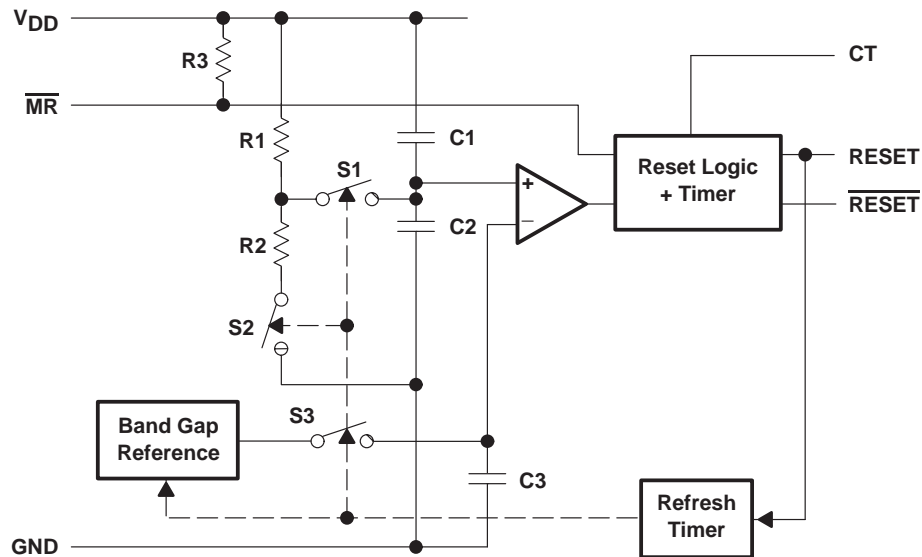


Figure 3. Block Diagram of the Supply Voltage Supervisor TPS383x

As already mentioned, the designer incorporated extremely low current consumption when developing this supply voltage supervisor. Actually, modern voltage monitoring devices using CMOS technology already show a very low supply current of $I_{DD} = 10 \mu\text{A}$ typically. For many applications, that is already a sufficiently small value. However, if systems work over a long period powered by the energy stored in one small battery, the user demands lower current consumption.

For this reason, several measures not normally found in such integrated circuits were necessary. Among these measures are the switches S1, S2, and S3 in figure 3. After turning on the supply voltage, these switches are closed. The voltage divider R1/R2 and the band gap reference are active. The voltage divider is responsible for the largest amount of the supply current of the device. Therefore, the refresh timer deactivates these elements whenever possible. The oscillogram in Figure 4 explains the refresh timer in detail. In Figure 4, the supply voltage V_{DD} rises starting at 0 V. As long as this voltage is smaller than the threshold voltage V_t ($\approx 0.5 \dots 0.6 \text{ V}$), the MOS transistors of the integrated circuit stay off. The supply current of the circuit is zero. When the supply voltage passes the value V_t , the circuit begins to work. Accordingly, the supply current increases with the rising supply voltage. At $V_{DD} \approx 1.4 \text{ V}$, the circuit has reached its final operating range. The supply current now amounts to approximately $I_{DD} = 8 \mu\text{A}$. With a further increase of the supply voltage, the voltage divider R1/R2 mainly determines the increase of this current. When the supply voltage becomes greater than the value $V_{IT+} = V_{IT-} + V_{hys}$, (see Table 3) the timer in the reset logic starts. This causes another rise in the supply current of approximately $2 \mu\text{A}$. After the delay time t_d is elapsed, the output $\overline{\text{RESET}}$ switches from low to high (into the inactive state). Simultaneously the refresh timer opens the switches S1 to S3 and switches off the reference voltage generator. The current consumption sinks to a few 100 nA. During the sleep mode, the comparator stays active monitoring the supply voltage through the capacitive voltage divider C1 and C2, while the accurate band gap voltage is stored in capacitor C3.

Every 60 ms from this point, the refresh timer wakes up the voltage divider and the band gap reference for 100 μ s. This process compensates leakage losses in the capacitors C1, C2, and C3. Figure 5 shows the increase of the supply current of about 10 μ A during this refresh cycle. When the refresh circuit is turned on or off, one observes a short increase of the supply current beyond the just-named value. This phenomenon is caused by the charge and discharge processes (current spikes, see section 4.2) in the circuit.

The capacitive voltage divider C1/C2 couples every supply voltage change into the noninverting input of the comparator. If at later time, the supply voltage V_{DD} sinks below the value V_{IT-} (see Figure 4), the comparator triggers the reset logic that activates the $\overline{\text{RESET}}$ output ($\overline{\text{RESET}} = \text{Low}$) again. Simultaneously, the refresh logic brings all parts of the circuit previously deactivated into the active condition. The supply current rises to $I_{DD} = 8 \mu\text{A}$.

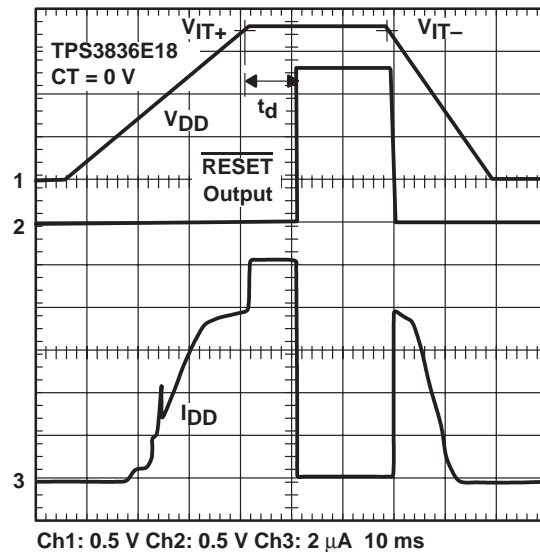


Figure 4. Output Signal and Supply Current of the Supply Voltage Supervisor

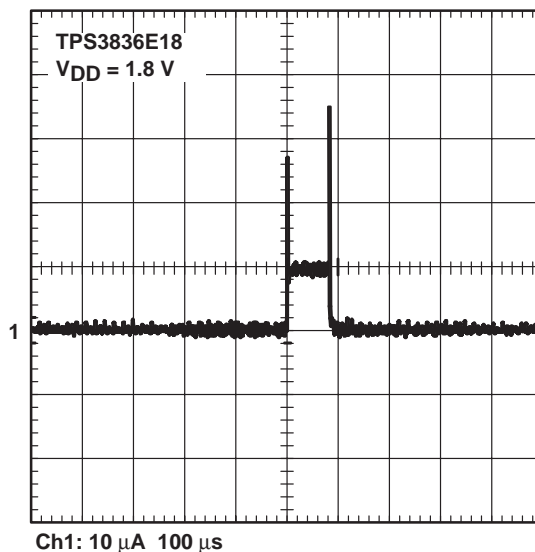


Figure 5. Supply Current During the Refresh Cycle

2.2 Circuit Versions

For circuits like the supply voltage supervisors described here, the 5-pin SOT23 package is of great advantage due to the low space required. However, the limited number of pins will not allow the RESET and $\overline{\text{RESET}}$ output to be available simultaneously. Therefore, the user must choose between the two versions, that in the active condition provide either a high or a low level. In some applications, like in section 3.2 and 3.4, an open drain configuration at the output is an advantage over a push-pull output. A corresponding version supports this need (see Table 1).

Table 1. Version of the Supply Voltage Supervisor

TYPE	OUTPUT			
	RESET	$\overline{\text{RESET}}$	PUSH-PULL	OPEN DRAIN
TPS3836		√	√	
TPS3837	√		√	
TPS3838		√		√

Figure 6 shows the pin-out of the various versions.

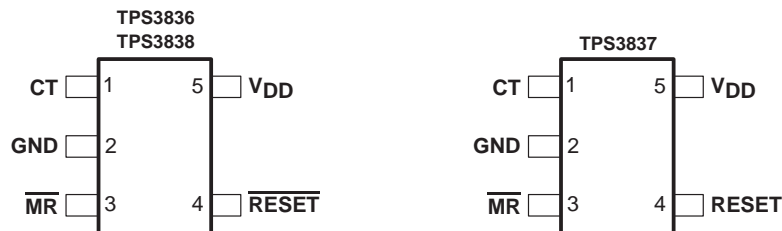


Figure 6. Pin Out

2.3 Function of the Device

The pulse diagram in Figure 7 explains the function and the temporal contexts by using the supply voltage supervisor TPS3836 as an example. In accordance with Figure 7, the supply voltage V_{DD} rises slowly starting from 0 V. When at time A in Figure 7, it reaches a typical amplitude of 0.6 V, the data sheet value is at most 1.1 V, and the circuit becomes active and switches the $\overline{\text{RESET}}$ output to a defined low level. It is assumed that the voltage at the input $\overline{\text{MR}}$ follows the supply voltage. At time B, the supply voltage reaches the value V_{IT+} . This voltage, divided by the voltage divider $R1/R2$ in Figure 3, exceeds the threshold of the comparator. The delay time t_d begins. After the delay time elapses, the output $\overline{\text{RESET}}$ becomes high again.

At time C, the output $\overline{\text{RESET}}$ becomes low because a signal source switched the input $\overline{\text{MR}}$ to low. After the signal at this input becomes high again, the delay time t_d starts. At the end of the delay the output $\overline{\text{RESET}}$ again switches to high.

By adding a large load to the output of the power supply shortly before time D for example, the supply voltage V_{DD} drops and falls below the threshold voltage V_{IT-} at moment D. The output $\overline{\text{RESET}}$ becomes active low. Thereafter, the supply voltage recovers and exceeds the threshold voltage V_{IT+} at time E. Again delayed by the time t_d , the output $\overline{\text{RESET}}$ returns to the high state.

Finally at time F, the equipment or a part of it is turned off. As a result, the supply voltage drops and the voltage monitor reacts. The output $\overline{\text{RESET}}$ now remains active until the voltage V_{DD} falls below 1.1 V (typically 0.6 V). Below this voltage value, the function of the circuit ceases and the output level may become undefined.

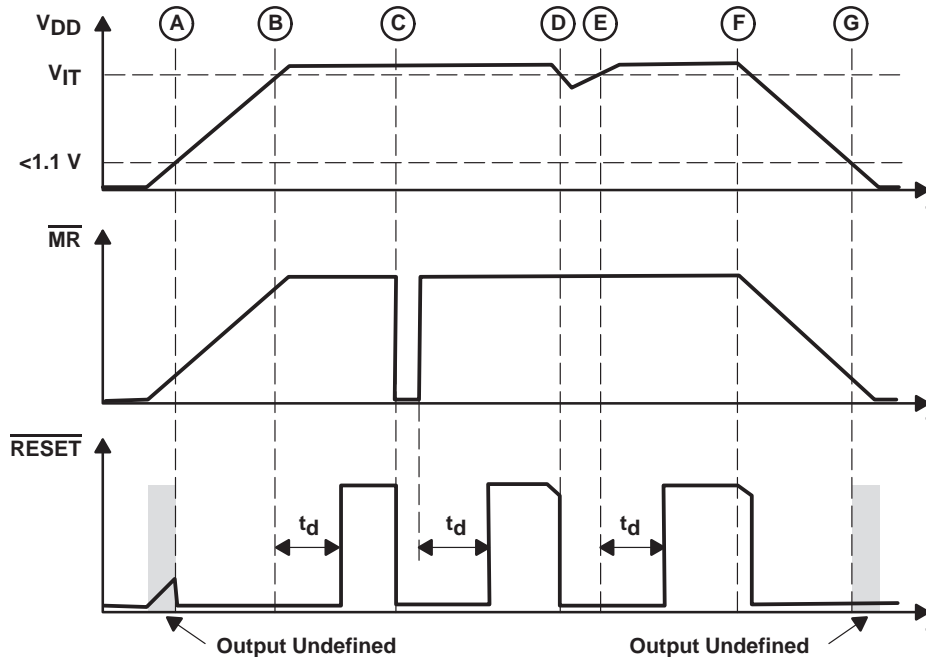


Figure 7. Timing of the Output Signal at the TPS383x

Figure 9 to Figure 12 show signals measured at the outputs of the integrated circuits TPS3836 and TPS3837 respectively. Figure 8 represents the setup used for these measurements. The generator powers the V_{DD} terminal of the device under test. The switch S1 applies a high (V_{DD}) or low level to the CT input and by that determines the length of the signal at the output $\overline{\text{RESET}}$ and $\overline{\text{RESET}}$ respectively (CT = Low: $t_d = 10$ ms; CT = High: $t_d = 200$ ms, see section 2.6). A 100-k Ω load at the output of the device under test forces this terminal in the first moment of the rise of the supply voltage to a logic level, which is opposite to the active level at this output. As shown in the following paragraphs, the user can determine at which supply voltage level the output becomes active and provides a defined level.

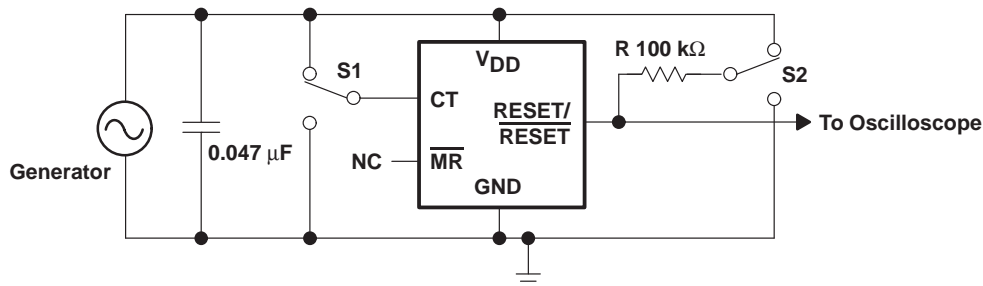


Figure 8. Measurement Setup

In Figure 9, the supply voltage (V_{DD}) rises from 0 V to its nominal level of 1.8 V in approximately 12 ms. The transistors inside the integrated circuit remain off until the supply voltage (V_{DD}) reaches a value that is greater than the threshold voltage (V_t) of the MOS transistors. During this phase, the voltage at the output $\overline{\text{RESET}}$ follows the level at the V_{DD} terminal due to the effect of the resistor (R) in Figure 8. When the supply voltage exceeds a value of approximately 0.6 V, ($V_{DD} > V_t$), the transistors inside the integrated circuit become active. From now on, the outputs occupy a defined state. The supply voltage exceeds the value V_{IT+} , the delay time (t_d) begins. Approximately 10 ms to 200 ms later, the output $\overline{\text{RESET}}$ switches to high.

The resistor (R) mentioned previously does not normally exist in an actual circuit design. However, in most cases the parasitic capacitance of the circuit assembly holds the voltage at the reset output at a value of 0 V during the turnon phase (see Figure 4).

Frequently, the system designer asks for supply voltage supervisors that provide a defined output signal with very small supply voltages, $V_{DD} = 0\text{ V}$ if possible. The designer of these integrated circuits cannot realize this request. For a circuit to function, a supply voltage V_{DD} is required which is greater than the threshold voltage V_t of the MOS transistors. As the following figures show, the output of the monitoring device provides a defined state when the supply voltage exceeds a value of 0.6 V.

However, a defined output signal of the monitoring circuit is conditioned to the correct initialization of the following circuit. A further condition is that the circuit to be initialized is in a position to understand the output signal of the supply voltage supervisor. Section 2.6 discusses this problem in more detail. Only if both conditions are met can the user expect the desired behavior from the setup.

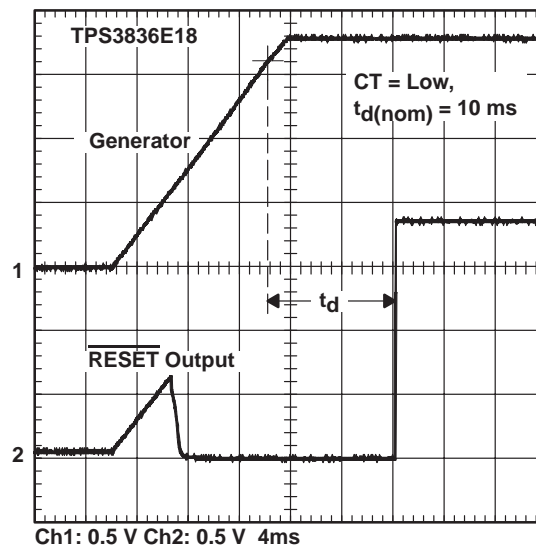


Figure 9. Output Signal TPS3836E18, CT = Low, $t_d(\text{nom}) = 10\text{ ms}$

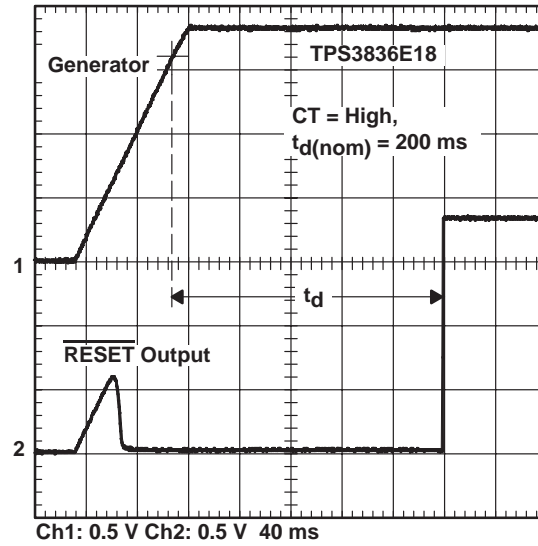


Figure 10. Output Signal TPS3836E18, CT = High, $t_d(\text{nom}) = 200 \text{ ms}$

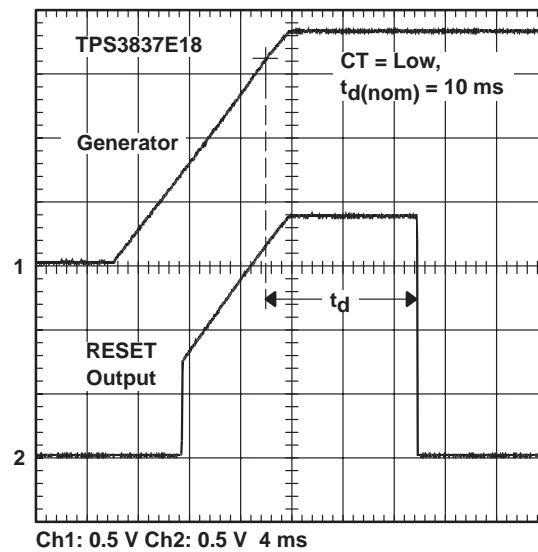


Figure 11. Output Signal TPS3837E18, CT = Low, $t_d(\text{nom}) = 10 \text{ ms}$

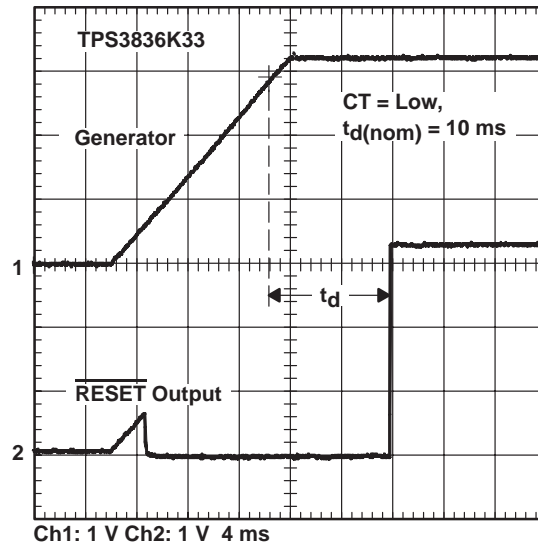


Figure 12. Output Signal TPS3836K33, CT = Low, $t_d(\text{nom}) = 10 \text{ ms}$

2.4 Threshold Voltage of the Supply Voltage Supervisor

The supply voltage supervisors described here display the proper operation of the power supply. Primarily of interest is a drop in this voltage, where the supply voltage falls under the minimum value required for a proper operation of the circuit. In the data sheets of the integrated circuits, this minimum value is designated: $V_{CC(\text{min})}$ or $V_{DD(\text{min})}$. This value takes the most unfavorable operating conditions into account:

- Process related deviations of the transistor parameters to the unfavorable side: with MOS transistors a high on-resistor, with bipolar transistors a low current gain.
- Unfavorable ambient temperature for the respective circuit: with MOS transistors a high value, that causes a high on-resistor of the device, with bipolar transistors a low temperature, that has a low current gain as the consequence.
- Highest possible clock frequency of the circuit, which presupposes the optimum performance of the transistors.

Under these conditions, the data sheets specify a minimum operating voltage that, with logic circuits, lies 10% below the nominal value. Complex MOS circuits, like microprocessors, demand a supply voltage that falls below the nominal value by no more than 5%. However, a 10% undervoltage can usually be tolerated in these cases. In rare cases, all of the mentioned operating parameters are the worst case. Mindful of these considerations, supply voltage supervisors where the threshold voltage (V_{IT-}) lies 10% below the nominal supply voltage are offered.

Based on these points of view, the threshold voltages (V_{IT-}) of the integrated circuits of the series TPS383x were selected (see Table 2).

Table 2. Threshold Voltage of the Supply Voltage Supervisors

TYPE	NOMINAL SUPPLY VOLTAGE V_{DD}	THRESHOLD VOLTAGE V_{IT-}	UNDERVOLTAGE %
TPS383xE18	1.8 V	1.71 V	5
TPS383xJ25	2.5 V	2.25 V	10
TPS383xL30	3.0 V	2.64 V	12
TPS383xK33	3.3 V	2.93 V	11

In order to prevent a consecutive and repeated response of the monitor circuit with low periodic fluctuations of the supply voltage (V_{DD}), the comparator has a hysteresis of a few millivolts (see Table 3). In practice, the low-pass characteristic produced by the delay circuit following the comparator will probably prevent a repeated reaction of the device under the just-mentioned circumstances. In this case, the output is held continuously active by the consecutive retrigger of the reset timer.

Table 3. Typical Hysteresis of the Threshold Voltage, V_{IT-}

NOMINAL THRESHOLD VOLTAGE V_{IT-}	TYPICAL HYSTERESIS V_{hys}
$1.7\text{ V} < V_{IT-} < 2.5\text{ V}$	30 mV
$2.5\text{ V} < V_{IT-} < 3.5\text{ V}$	40 mV
$3.5\text{ V} < V_{IT-} < 5.0\text{ V}$	50 mV

2.5 Length of the Reset Signals

The integrated circuits described here will recognize voltage drops of the supply voltage that can endanger the reliable operation of the circuit. To assess the amplitude and duration of these voltage drops and to judge the effectiveness of the monitoring device, the user must analyze the cause. Voltage drops of the supply voltage have two essential causes:

- Extreme load variations that cannot be stabilized by the voltage regulator sufficiently or quickly or cannot be stabilized at all.
- Voltages that are coupled from external noise sources into the system. These disturbances come from electrostatic discharges, arcs, inductive loads, and sometimes lightning impacts during a thunderstorm. They sometimes distinguish themselves through extremely high energies.

2.5.1 Supply Voltage Drops Due to Load Variations

In order to exploit the energy stored in a battery as completely as possible, low-dropout voltage regulators are used in these applications. The amplifiers integrated in such regulators in combination with the pass element have a settling time of several ten microseconds as shown in Figure 13. The voltage monitor device must recognize a drop under the minimum specified supply voltage caused by the discharge of the battery. Also, this circuit must recognize inadmissible voltage drops caused by load variations. Therefore, the user demands a reaction time of such a device in the microsecond range.

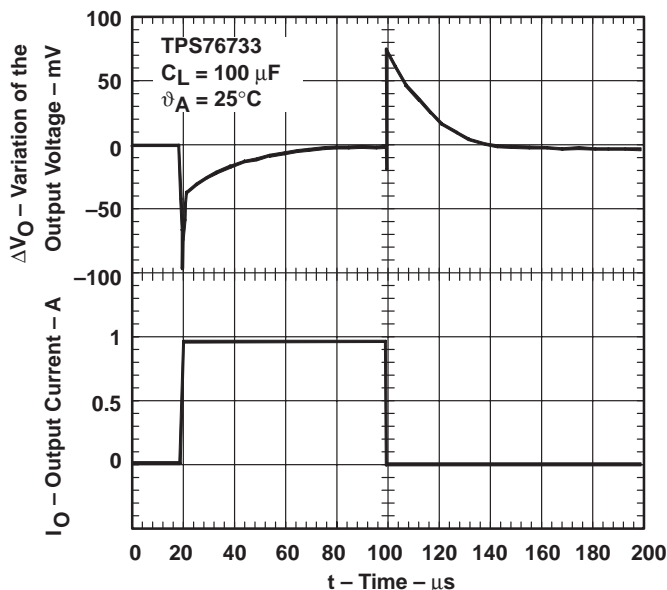


Figure 13. Supply Voltage Drops Due to Load Variations

2.5.2 Influence the Supply Voltage Through External Noise Sources

The estimation of the consequences of disturbances that comes from external noise sources is more difficult. Such sources could be:

- Electrostatic discharges have an amplitude of several thousand volts. Due to the limited amount of energy in the discharge, e.g. the energy stored in a human body, such discharges last only a few nanoseconds. Admittedly, the amplitude of the discharge is very high. The inductance of the interconnects quickly damps the wave propagating from the point of discharge. Even if the discharge is very dangerous for the integrated circuits, it is questionable whether a signal is sufficient enough to appear at the sense input of the supply voltage supervisor.
- The user has to consider that the application area of the monitor device described here is mainly in battery-operated equipment. With these applications, the user can assume in many cases that the monitored circuit has no galvanic connection to the outside world. With a sufficient isolation of the equipment against an unintentional touch of sensitive components, one can prevent high currents flowing through critical parts of the system.
- Lightning is among the electrostatic discharges. The duration of such discharges is so big that monitoring circuits can recognize the resulting supply voltage drops. Experience teaches, however, that the induced energy may be so high that it probably will destroy the circuit.

Among the high-energy disturbances are those that come from powerful electric equipment like big motors and transformers. The simplified waveform of such disturbance is shown in Figure 14. The amplitude of such an impulse is in the order from several hundred to several thousand volts. The rise time (t_r) amounts to 100 ns to 1000 ns, while the fall time (t_f) with 10 μ s to 100 μ s is relatively long.

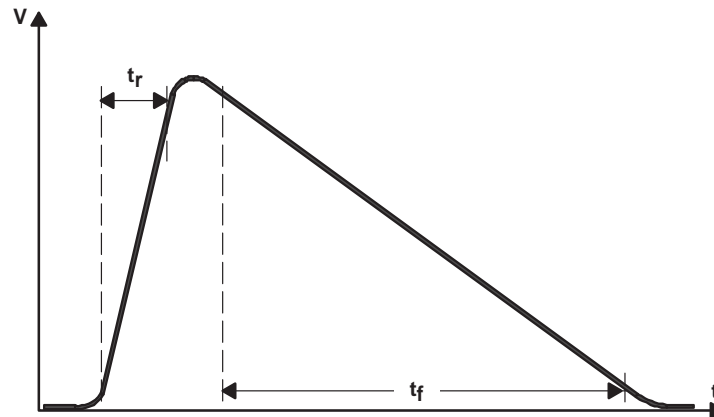


Figure 14. Waveform of a High-Energetic Disturbance

The coupling path between noise sources and noise destination influences the actual effective form and amplitude of the impulse. In practice, the user must calculate a pulse-width in the microsecond range with insufficient decoupling or poor shielding.

Concerning the possible influence of these disturbances on battery-operated equipment, it is valid to refer to the preceding text on electrostatic discharges. As long as the circuit does not have any electric connection to the outside world, the previously mentioned disturbances will have no influence on the function of the appliance. However, any electric connection to the outside world represents a probable noise path. This is also valid for galvanic isolated connections. The inherent existing stray capacitance of the interface is a possible path for the disturbing signals.

2.5.3 Behavior of the Supply Voltage Supervisor TPS383x

Supply voltage supervisors will recognize a deviation in the supply voltage from its nominal value and generate a signal when the voltage falls below the minimum acceptable value. These processes take place in the millisecond range. It is also necessary to recognize external disturbances, which influence the voltage supply, and to force a reinitialization of the system if required. In this case the monitoring circuit must recognize deviations in the microsecond range.

The reaction of the supply voltage supervisor TPS3836 on a short drop in the supply voltage for the duration t_W is shown in Figure 15. The version TPS3836K33 is intended for applications with a nominal supply voltage, $V_{DD(nom)} = 3.3 \text{ V}$. According to the data sheet, the threshold voltage is $V_{IT-(nom)} = 2.93 \text{ V}$. That means the device should react when the supply voltage deviates from the nominal value by:

$$V_{DD(nom)} - V_{IT-(nom)} = 3.3 \text{ V} - 2.93 \text{ V} = 370 \text{ mV}$$

As Figure 15 shows, this applies to voltage drops lasting longer than $20 \mu\text{s}$. With shorter voltage drops, the sensitivity decreases. Since an extreme sensitivity is usually not desired, the device is designed so that it will not recognize voltage drops shorter than $7 \mu\text{s}$.

Figure 15 also shows the behavior of the supervisor circuits TPS32836E18 ($V_{IT-(nom)} = 1.71 \text{ V}$) and TPS32836J25 ($V_{IT-(nom)} = 2.25 \text{ V}$). With a lower threshold voltage, the sensitivity against a short voltage sometimes increases slightly, e.g., the device to be used with a nominal supply voltage, $V_{DD} = 1.8 \text{ V}$, recognizes voltage drops of a duration down to $t_W = 3 \mu\text{s}$.

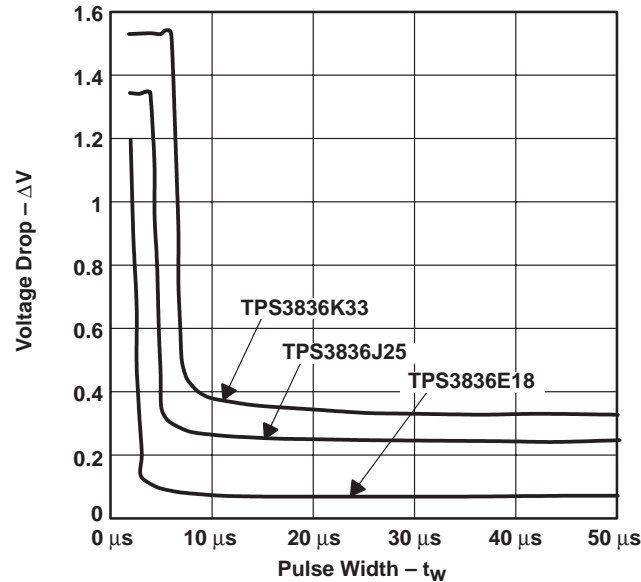


Figure 15. Reaction on Short Supply Voltage Drops

2.6 Length of the Reset Signals

One of the essential tasks of the supply voltage supervisors is to assure a correct initialization of the system. Integrated circuits require a reset signal of a specified length at its reset input. With logic circuits, this signal duration is in the range of a few nanoseconds. Complex integrated circuits like microprocessors execute during the initialization of a microprogram that brings the individual parts of the circuit sequentially into the desired state. The following conditions must be fulfilled in order to assure a correct result:

- The supply voltage must have risen at least to the voltage $V_{DD(min)}$, and $V_{CC(min)}$ respectively to assure the correct function of the total circuit.
- The clock generator (oscillator) of the circuit to be initialized must work correctly in order to assure the execution of the microprogram.
- The reset signal must last until the successful completion of the initialization.

The comparator in the supply voltage supervisor recognizes the achievement of a sufficient supply voltage, point B in Figure 7. The execution of the microprogram lasts approximately 100 ns up to a few microseconds; the exact value is found in the data sheet of the corresponding circuit. Essentially, it often lasts until the oscillator of the circuit works correctly. Clock generators are usually crystal-controlled. Crystals are components with a very high quality ($Q > 10^4$). With the correct dimensioning of this circuit, the settling time of the oscillator lasts up to several ten milliseconds (see section 3.1). For this reason, the delay time (t_d) of the supervision circuits normally amounts to approximately 100 ms. With the integrated circuit of the series TPS383x discussed here, this value amounts to $t_{d(typ)} = 200$ ms.

Many applications ask for a real-time clock that runs in the standby mode. Due to cost and performance reasons, the frequency of these oscillators is mainly controlled by watch crystals ($f = 32.768 \text{ kHz}$). For cost reasons, this signal serves as a time base for the clock generator of the processor itself. It is a voltage-controlled ring-oscillator in which frequency is controlled via a phase-lock loop (PLL) to the multiple frequencies of the watch crystal. These ring-oscillators have a settling time of a few periods only. After this time the processor is able to function even if the frequency is not correct until the final settling of the PLL. Under such circumstances, the user can shorten the length of the reset signals.

With the supervision circuit of the TPS383x, the user has the ability to select the appropriate delay time via a corresponding logic level at the CT input (see Table 4).

Table 4. Length of the Reset Signals

INPUT CT	LENGTH OF THE RESET SIGNALS
High	200 ms
Low	10 ms

3 Application Examples

3.1 Digital Sensor Signal Processor With One Supply Voltage

The application of the supply voltage supervisor described here is very simple. Figure 16 shows the use of this circuit in context with the digital sensor signal processor MSP430C1111. The wide supply voltage range of this device ($V_{CC} = 2.2 \dots 3.6 \text{ V}$) allows the operation without an additional voltage regulator. Due to the extremely low supply current of $I_{CC} = 160 \mu\text{A}$ at a clock frequency of 1 MHz at a supply voltage $V_{DD} = 2.2 \text{ V}$ and only $I_{CC} = 0.8 \mu\text{A}$ in the standby mode, this circuit finds uses in applications in which the equipment should work with one battery over years. Examples are portable measuring instruments. Under these conditions, the current consumption of the supply voltage supervisor must be of no consequence. The integrated circuits of the series TPS383x, which show a supply current of $I_{DD} = 250 \text{ nA}$ in the normal operation, are the ideal device in these applications.

As Figure 16 shows, the application of these integrated circuits is straightforward. A single lithium battery is the energy source for the sensor signal processor as well as the monitoring circuit. The output **RESET** (active low with low battery voltage) directly controls the reset input **RST** of the processor. If required, the pushbutton switch (S) at the input (**MR**) activates the initialization of the circuit. If this switch is opened, the pullup resistor integrated into this input provides a defined logic level (high).

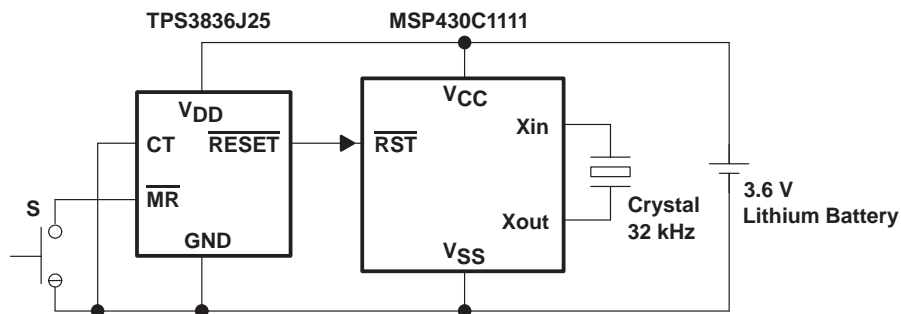


Figure 16. Voltage Monitor for the Sensor Signal Processor MSP430

The logic level at the entrance CT of the supply voltage supervisor determines the length of the reset signals. The clock generator of the signal processor consists of a programmable ring oscillator, the frequency of which may be set to $f = 1$ MHz. The crystal serves as the time basis for the integrated real-time clock and supports the extremely low current consumption of the processor in the standby mode (clock generator turned off). The ring oscillator in the clock generator, which controls the operations of the processor, has a settling time that lasts only few periods of this oscillator. Accordingly the user can choose the delay time of the supply voltage supervisor. For this reason, in Figure 16, a low level is applied to the CT input. This yields a delay time $t_d = 10$ ms (see Table 4).

3.2 Digital Signal Processor With Two Supply Voltages

Advanced high-performance processors like the digital signal processor of TMS320VC33 operate in its kernel with supply voltages of only 1.8 V. The low voltage supports the need for reduced field strengths that the small geometries in the integrated circuit request. Simultaneously, this measure allows a significant reduction of the power dissipation of the circuit. Other devices connected at the signal processor, e.g. memories, usually require a higher supply voltage. For this reason, the interface of such processors is designed so that it can run with a supply voltage $V_{DD(P)} = 3.3$ V. In this case, the user must monitor both voltages $V_{DD(L)}$ and $V_{DD(P)}$ of the processor. Two supply voltage supervisors are provided in the example in Figure 17.

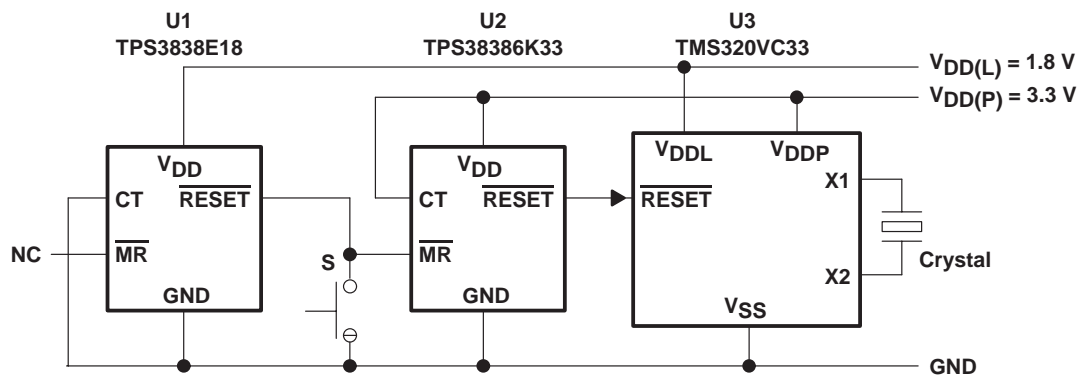


Figure 17. Supply Voltage Supervisor for a Processor With Two Supply Voltages

The circuit U1 (TPS3838E18) monitors the supply voltage of the processor kernel $V_{DD(L)}$ (nominal 1.8 V). The output $\overline{\text{RESET}}$ of this device is an open-drain output. This terminal directly controls the input $\overline{\text{MR}}$ of the following circuit (TPS3836K33), which monitors the supply voltage $V_{DD(P)} = 3.3$ V. The open-drain output allows a simple level conversion from 1.8 V (TPS3838E18) to 3.3 V (TPS3836K33). The pullup resistor integrated in the input $\overline{\text{MR}}$ of U2 takes care of a correct high level. The output of the circuit (U2) controls the input $\overline{\text{RESET}}$ of the processor (TMS320VC33). Parallel to the input $\overline{\text{MR}}$ of the circuit (U2) is the pushbutton switch (S). An activation of this switch causes an initialization of the system.

Finally, the logic levels at the inputs (CT) have to be determined. The logic levels determine the length of the reset signals. The processor (TMS320VC33) has an integrated crystal oscillator (terminals X1 and X2). For the correct initialization of the processor, a sufficient amplitude of the oscillator voltage is necessary. As mentioned in section 2.6, the settling time of correctly dimensioned crystal oscillators last several 10 milliseconds. Therefore, the user chooses a value of 200 ms as the reset time of the circuit, U2 (CT = high). Now the only task of the circuit (U1) is to monitor the supply voltage $V_{DD(L)}$. In principle a simple comparator function would be sufficient for this task. A timing extension of the reset signals is not necessary. Therefore, a low level at the input (CT) of this circuit selects the shorter of the two delay times.

3.3 Circuits With Active-High Reset Input

Most microprocessors, microcomputers, and logic circuits request a reset signal that is active low, as in Figure 16 and Figure 17. However, some circuits request a high level at the reset input in order to execute the reset function: some CMOS logic circuits of the series CD4000 and the microcontrollers of the series 80xx are offered by various manufacturers. Figure 18 shows the application of the supply voltage supervisor TPS3837 with such a microcomputer.

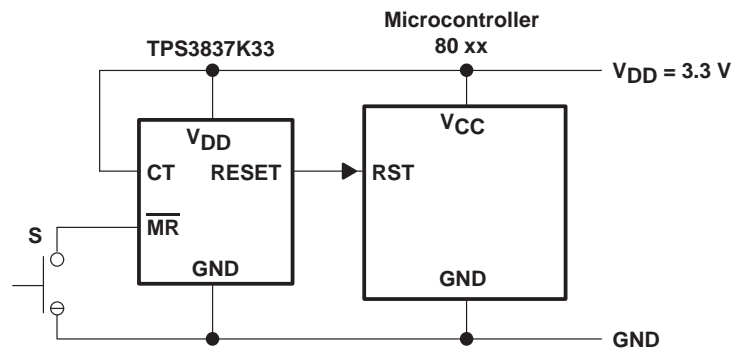


Figure 18. Initialization Circuit for a Microcomputer With Active-High Reset Input

3.4 Microcontrollers With Bidirectional Reset Port

Some microcontrollers, like the series MC68HC05, possess a bidirectional reset terminal. A low level at this input causes an initialization of the circuit as described previously. Additionally such a controller itself is capable of switching this terminal to low. This feature is used to force peripheral circuits, software controlled, into an initial state. To enable the reset function by two sources (supply voltage supervisor and the microcontroller) a monitoring device with an open drain output is required, as in the case with the version TPS3838. An additional pullup resistor (R) in Figure 19 provides a defined high level.

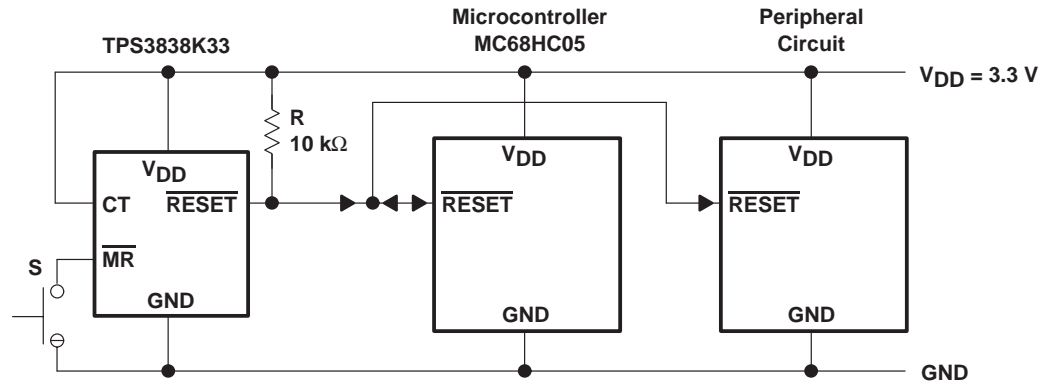


Figure 19. Reset Circuit for a Microcontroller With Bidirectional Reset Terminal

3.5 Monitoring of Positive and Negative Supply Voltages

Many analog circuits require both a positive and a negative supply voltage, e.g. 3.3 V and -3.3 V. If both voltages are available, most operational amplifiers can process dc voltages with positive and negative polarity. In such cases, the monitoring system has to sense both voltages. This is possible with the appropriate arrangement, as Figure 20 shows.

The example (see Figure 20) shows a circuit proposal for monitoring two voltages $V_{CC1} = 3.3$ V and $V_{CC2} = -3.3$ V. The circuit, U2 (TPS3836), senses positive supply voltage V_{CC1} , while the other circuit, U1 (TPS3837), senses the negative voltage V_{CC2} . The level translation on the -3.3 V referenced output signal of U1 to a level referenced on 0 V is done by the field-effect transistor, Q (SST201, manufacturer Siliconix). With an inadequate value of V_{CC2} , the output RESET of the circuit (U1) is high = 0 V. Therefore, the gate-source-voltage V_{gs} of the transistor (Q), is 0 V. The transistor is on and applies a low level to the input (\overline{MR}) of the circuit (U2). This condition, as well as a insufficient amplitude of V_{CC1} , results in a low level at the input (RESET) of the microcontroller. The usage of the N-channel FET (Q) ensures a valid output signal for the monitoring arrangement even if the voltage at V_{CC2} fails totally.

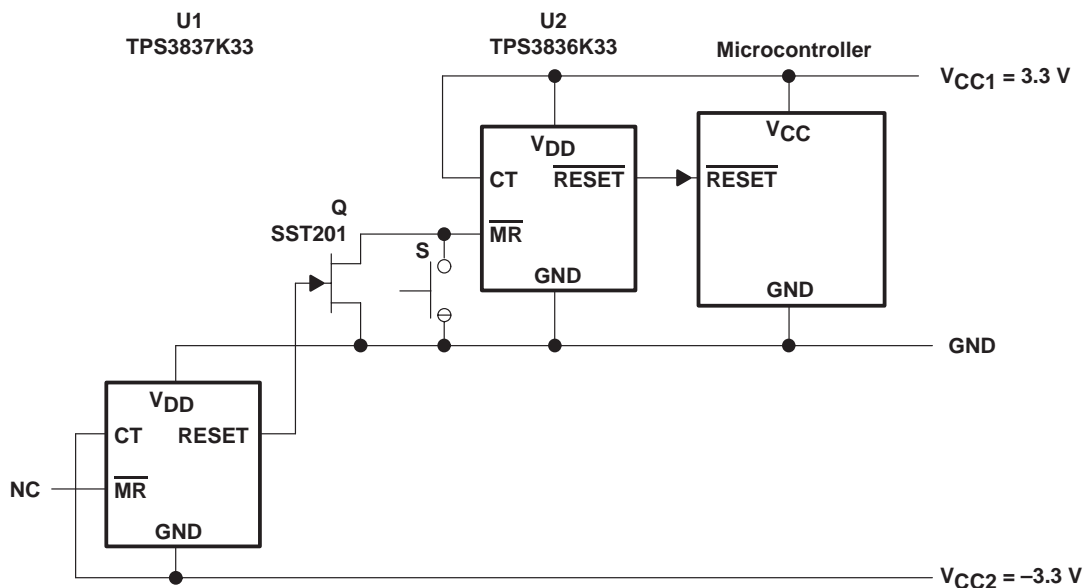


Figure 20. Monitoring a Positive and Negative Supply Voltage

3.6 Debouncing of Switches

Other applications can use supply voltage supervisors. A frequently occurring problem is the debouncing of mechanical contacts. If the contact surface clashes with the closing of the contact, it bounces back several times. A similar effect is observed later when opening the contact. According to the construction of the contact, this bounce period lasts in the range from hundreds of microseconds to tens of milliseconds. In the comparison to the reaction speed of digital circuits, it is a very long period, so the bouncing of the contact is interpreted as multiple events.

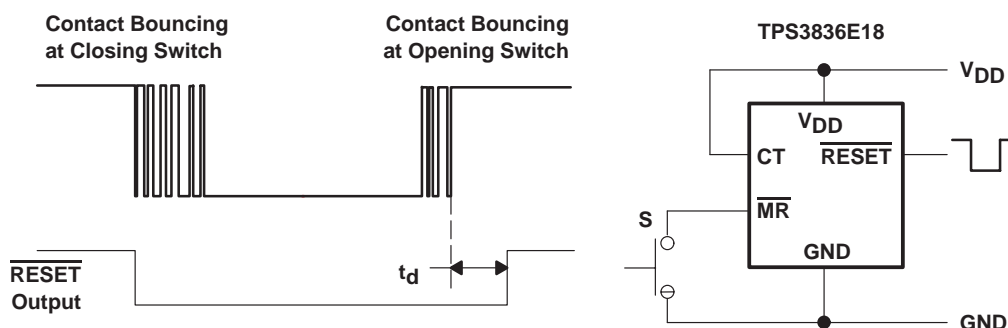


Figure 21. Debouncing a Contact

A known circuit arrangement to debounce a contact consists of a low-pass filter followed by a Schmitt-trigger. These functions comprise the supervisor circuits. When activating the pushbutton switch (S) in Figure 21, the input (\overline{MR}) becomes low. The output (\overline{RESET}) follows this signal. The low level at the input simultaneously activates the reset timer (see Figure 7) that keeps the output, an additional 200 ms, in the active mode after a positive edge at the input (\overline{MR}). This provides the low-pass characteristic that fades multiple pulses caused by the bouncing contact. The same happens when opening the contact. When selecting a suitable integrated circuit for debounce purposes, the user has to look for a device whose threshold voltage (V_{IT-}) is much lower than the minimum supply voltage of the system. Therefore, a circuit with a threshold voltage of $V_{IT-} = 1.71\text{ V}$ is used in this example with a supply voltage of $V_{DD} = 3.3\text{ V}$. This way, the user prevents small supply voltage drops that may cause an unintended reaction to the debounce circuit.

4 Design Hints

4.1 Printed-Circuit Board Layout Considerations

As the examples in section 3 showed, the use of the supply voltage supervisors is very simple. The different versions of this circuit, which provide either active high or low output, and the additional input \overline{MR} support various applications.

Nevertheless, the designer should pay attention to some rules when using these devices in order to avoid unpleasant surprises. The supply voltage supervisors best suited for usage in digital applications appear at first to be digital circuits. Actually, these modules contain, as shown above, sensitive analog circuits: the reference voltage source and the comparator. Moreover, these integrated circuits are selected according to their application so that their threshold voltage (V_{IT-}) differs only a few percent from the nominal supply voltage of the system. Their task is to recognize abnormal drops in the supply voltage. The designer must prevent the short term noise, originated by the operation of the system, that causes a reaction to the circuit.

In many cases, ground bounce is the cause for such noise in the system. This noise is generated by fast and large current changes. The sources of these currents are, for example, multichannel bus interface circuits. Besides eight-, sixteen-, or 32-channel logic circuits, the bus interface circuits of microprocessors belong to this category. Also, loads are to be named at this point which handle big currents like filament lamps (turn on current) or electric motors. In most cases, nothing can be done about the currents themselves. They are necessary to fulfil the function of these components. However, the designer can be concerned with the careful placement of the modules, so that these excessive currents and voltages cannot effect the supply voltage. Among these measures, the monitoring circuit must be placed primarily on the printed-circuit board where the disturbances appear in a low degree or not at all.

Another measure to avoid an unwanted reaction of the supply voltage supervisor, is the careful layout of the printed-circuit board (see Figure 22). The blocking capacitor (C) is placed parallel to the supply voltage. No other currents of the system must be allowed to flow on the interconnects between this capacitor and the integrated circuit. These currents may cause ground or supply line (V_{DD}) bounce that superimposes the voltage to be monitored and leads to an unintentional triggering of the circuit.

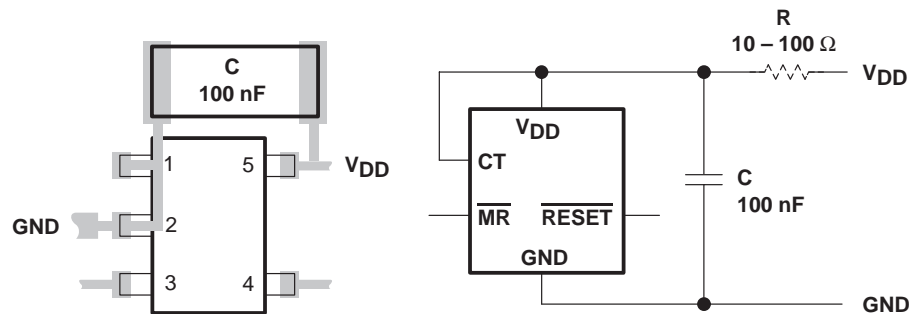


Figure 22. Proposal for the Printed-Circuit Board Layout

The capacitor (C) has multiple tasks. First, it provides a low impedance of the power supply at high frequencies, and this prevents an unintentional feedback in the analog parts of the device in question. Second, this capacitor delivers the energy required for the current spikes during the output's transition (see section 4.2). And third it delivers the energy required to charge the load capacitance.

In some cases a resistor (R) in the supply lines, in combination with the capacitor (C), may keep disturbances away from the circuit. Nevertheless, it is more meaningful to explore the cause of an unintentional reaction of the integrated circuit than to filter these disturbances without knowing their exact source. Disturbances may have their cause in the power supply itself. The current limiter of the voltage regulator may start too early, so that load changes lead to large drops of the supply voltage (see Figure 13). The selection of an appropriate voltage regulator is the better solution. Otherwise, the voltage regulator delivers too low a voltage that already lies close to the threshold voltage (V_{IT-}). A better adjustment of the output voltage of the regulator solves the problem.

4.2 Correct Input Levels

During the design of the integrated circuit, the designers were careful to maintain the low supply-current of the device. Therefore, the user of this module must watch that its good performance is not worsened by an improper operation of the circuit. The levels at the inputs (\overline{MR} and CT) are a critical point. The principal circuit diagram of the inputs is shown in Figure 23.

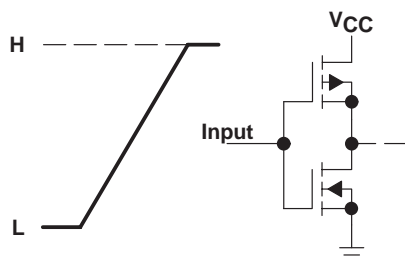


Figure 23. Input of a CMOS Circuit

As long as a high level ($= V_{DD}$) or a low level ($= GND$) is applied to the input of the circuit, either the P-channel or the N-channel MOS transistor is turned off. Consequently, no supply current flows through the circuit. This feature of the CMOS technique is responsible for the extremely low supply-current of these devices. However, with an input voltage of $V_t < V_{in} < (V_{DD} - V_t)$ (V_t = threshold voltage of the MOS transistor), both transistors are more or less conducting simultaneously. This characteristic is responsible for the current spikes that one observes with each transition (see Figure 5). In the present case, the threshold voltage amounts to $V_t \approx 0.6$ V. However, Figure 24 shows a supply voltage $V_{DD} = 3,3$ V. The current through the two transistors reaches its maximum value at $I_{DD} \approx 70$ μA , if the input voltage (V_I) is approximately half as high as the supply voltage (V_{DD}).

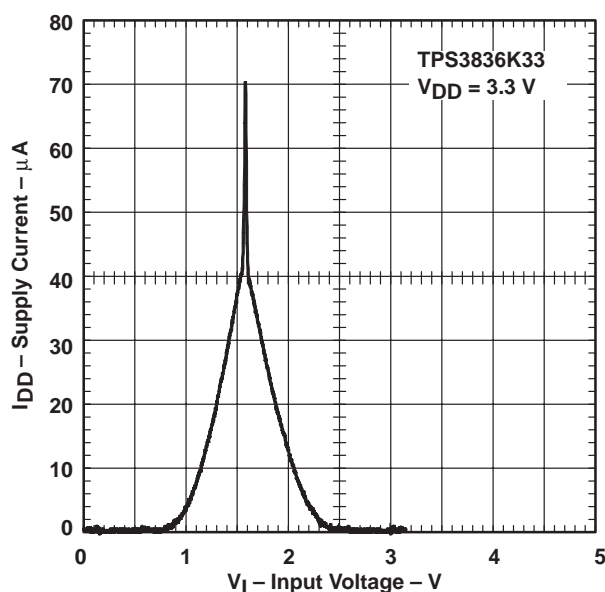


Figure 24. Supply Current of a CMOS Inverter

This situation is of no importance as long as the levels at the inputs hold one of the two transistors off. In most applications, the user will connect the CT input with one of the two supply voltage rails that assures the demanded levels. In case another signal source controls this input, the user must watch the correct levels. By no means, should an input be open. With high probability, leakage currents in the circuit generate an input voltage that leads to an increased supply current. This also applies to the input (\overline{MR}) that leads other signal sources in many applications, see Figure 17 and following. However, if this input is not connected, the pullup resistor integrated into this connection provides a defined high level.

5 Summary

The concept of electromagnetic compatibility is being discussed in the electronics industry. Usually the designer thinks of this expression as electromagnetic pollution or a similarly nebulous phenomena. The designer does not consider that often more trivial things influence the compatibility of a circuit or equipment. The reliable operation of a system falls under the concept of compatibility. In order to support this feature, Texas Instruments offers the supply voltage supervisors of the series TPS383x, which monitor important parameters of a system including the correct supply voltage. Digital circuits, like microprocessors and microcomputers, request an initialization after turning on the voltage supply. The described integrated circuits also adopt this task. A supply voltage of 1.8 V with a typical supply current of approximately 250 nA allows the use of these components, particularly in battery-operated sets. A series of various integrated circuits is available to the system designer that provides easy, simple, and advantageous solutions for the described tasks.

6 References

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3. Texas Instruments: data sheet TPS3801 (literature number SLVS219)
4. Texas Instruments: data sheet TPS3809 (literature number SLVS228)
5. Texas Instruments: data sheet TPS3823 (literature number SLVS165A)
6. Texas Instruments: data sheet MSP430C31 (literature number SLAS165C)
7. Texas Instruments: data sheet TMS320VC33 (literature number SPRS087)
8. *Supply Voltage Supervisor TL77xx Series Application Report* (literature number SLVAE04)
9. *The TPS370x Family Application Report* (literature number SLVA045)
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1. Texas Instrument: Linearly Design Seminar (literature number SLYD016)

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