

# National LVDS Products

Spring 2004

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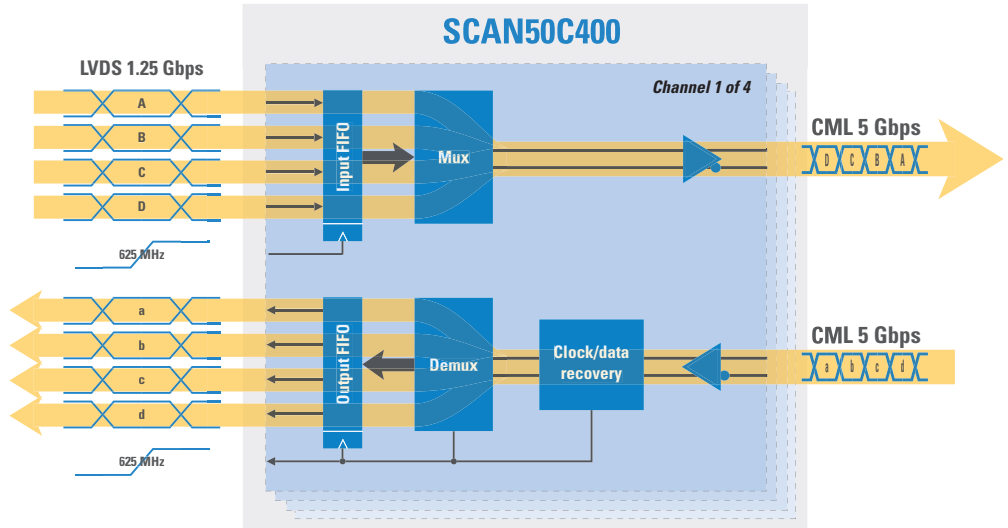
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## SCAN50C400

40 Gbps SerDes transceiver

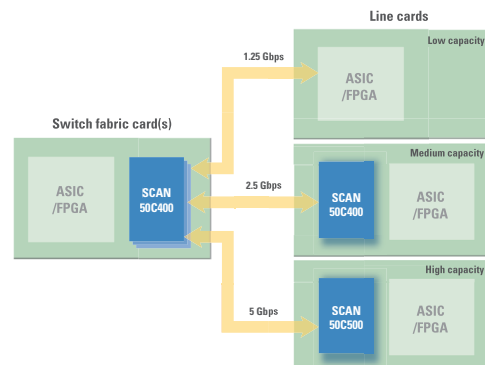


### Product description

The SCAN50C400 is a four-channel 5 Gbps serializer/deserializer transceiver providing an impressive 40 Gbps full duplex throughput. Each channel multiplexes four 1.25 Gbps LVDS serial streams into one 5 Gbps CML signal, quadrupling the capacity of FR4 backplane systems. In addition, the support of slower 2.5 and 1.25 Gbps rates allows backward compatibility to existing lower capacity sub systems. Better than  $10^{-15}$  bit error rate performance and a comprehensive suite of test modes make the SCAN50C400 ideal in high bandwidth, high reliability applications.

### Features

- Quad 5 Gbps SerDes for a total of 40 Gbps full duplex throughput
- Each channel supports 5, 2.5, or 1.25 Gbps rates
- Better than  $10^{-15}$  bit error rate over FR4 backplanes
- At-speed loopback and BIST test modes
- Configurable through IEEE P802.3ac-compliant MDIO interface
- On-chip LVDS and CML terminations
- 23 x 23 mm BGA package

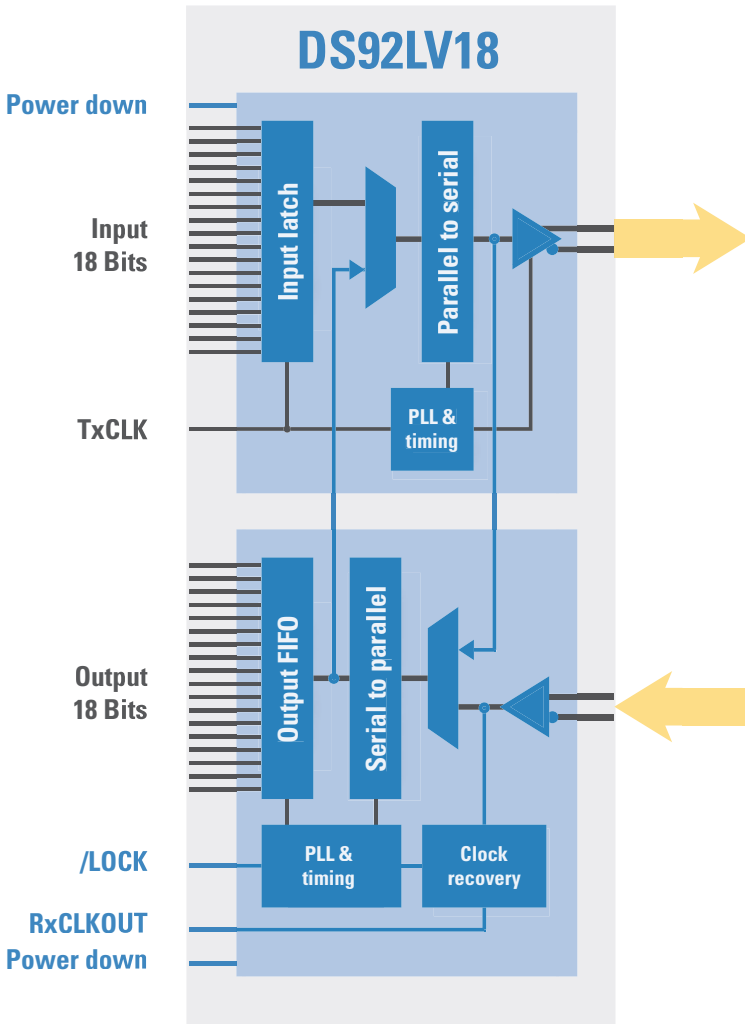


# Bus LVDS SerDes

Flexible and easy-to-use

## DS92LV18

18-bit, 15 - 66 MHz SerDes (270 - 1188 Mbps payload)



### Product description

The DS92LV18 serializes and deserializes up to 18 bits over a wide, 15 - 66 MHz clock range. The extra-wide 18-bit bus allows additional information such as parity, frame, sync, control, status etc signals to be serialized along with data. Integrated automatic receiver lock to random data capability allows true “plug & go” hot insertion capability without the need for special synchronization characters.

### Features

- 18-bit parallel bus interface (no external coding required)
- Wide 15 - 66 MHz clock range
- Automatic receiver lock to random data
- Transmitter and receiver can be operated independently
- Relaxed transmitter and receiver clocking requirements
- Local and remote loopback modes
- Industrial -40° to +85°C temperature range
- Single 3.3V supply
- 80-lead PQFP package

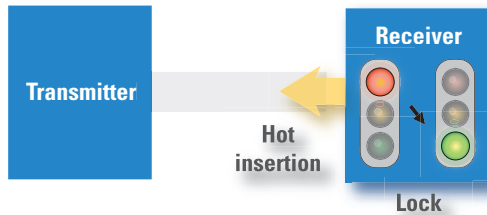
### Pricing (1k+ quantities)

- DS92LV18 \$9.95

## Other selected Bus LVDS SerDes

Part number	Bus width	Serializers	Deserializers	Speed
DS92LV16	16	1	1	25 - 80 MHz
SCAN921025	10	1	—	30 - 80 MHz
SCAN921226	10	—	1	30 - 80 MHz
SCAN928028	10	8	—	25 - 66 MHz
SCAN926260	10	—	6	25 - 66 MHz

### Automatic receiver lock to random data



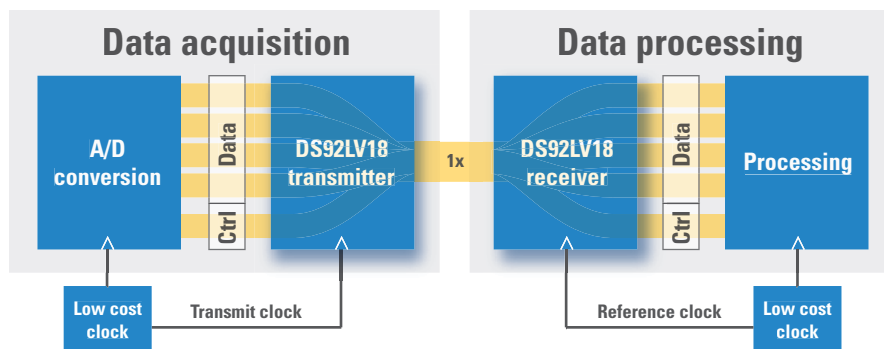
Automatic receiver lock to random data “plug & go” hot insertion capability eliminates the need to interrupt data traffic with training characters.

### Relaxed clocking

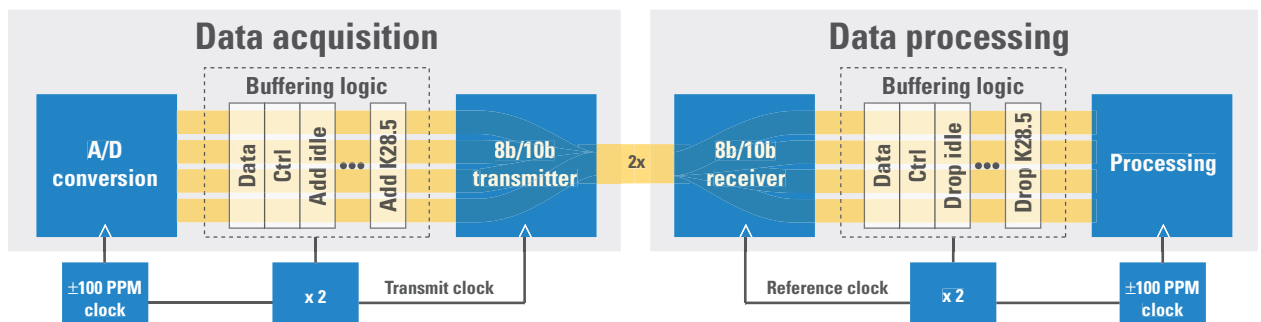
Parameter	8b/10b SerDes	Bus LVDS SerDes
Transmit clock jitter tolerance (RMS)	5 ps	80 or 120 ps
Transmit/receiver clock frequency disparity	± 100 PPM	± 50000 PPM

Relaxed clocking requirements lower the cost and complexity of clock distribution networks.

### Lower overhead



Many applications require the transmission of byte-oriented data plus some extra non-data information such as control, parity, frame/sync, interrupt, status, etc. Bus LVDS SerDes like the DS92LV18 easily serialize this extra information along with data.



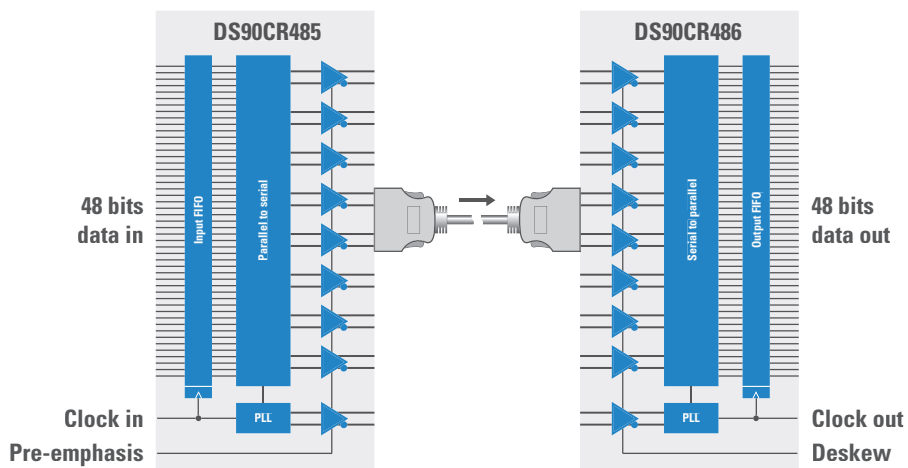
Other byte-oriented SerDes force the designer to buffer and packetize extra information, increasing logic overhead and serialization clock rate.

# Channel Link SerDes

For wide buses up to 48 bits

## DS90CR485/486

6.38 Gbps, 48-bit, 66 - 133 MHz SerDes



### Product description

The DS90CR485/486 Channel Link SerDes chipset serializes and deserializes wide LVTTTL buses up to 48 bits at parallel bus clock speeds from 66 to 133 MHz, providing up to 6.38 Gbps data payload throughput.

### Features

- Up to 6.38 Gbps data payload
- Serializes up to 48 bits over wide a 66 - 133 MHz clock range (no external coding required)
- Programmable transmitter pre-emphasis and DC balance drives cables up to 10m
- Automatic receiver cable deskew
- Low power
- 100-lead TQFP package

### Pricing (1k+ quantities)

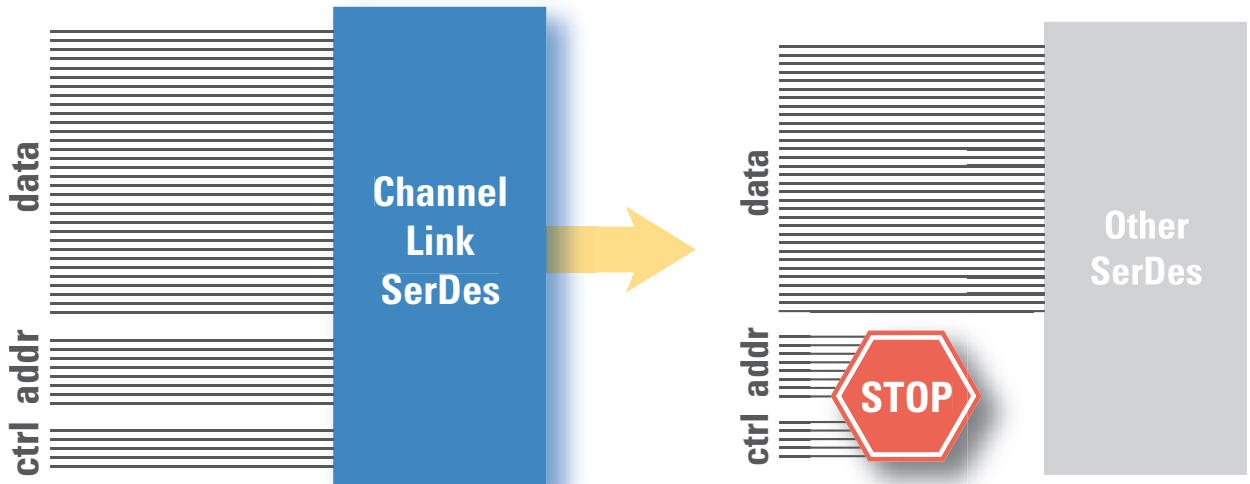
- DS90CR485 \$12.90
- DS90CR486 \$12.90

## Other selected Channel Link SerDes

Part number	Bus width	Bus speed	Max payload
DS90CR481/482	48	65 - 112 MHz	5.37 Gbps
DS90CR483/484	48	33 - 112 MHz	5.37 Gbps
DS90CR287/288A	28	20 - 85 MHz	2.38 Gbps
DS90CR217/218	28	20 - 85 MHz	1.78 Gbps
DS90CR285/286A	21	20 - 66 MHz	1.84 Gbps
DS90CR215/216A	21	20 - 66 MHz	1.38 Gbps

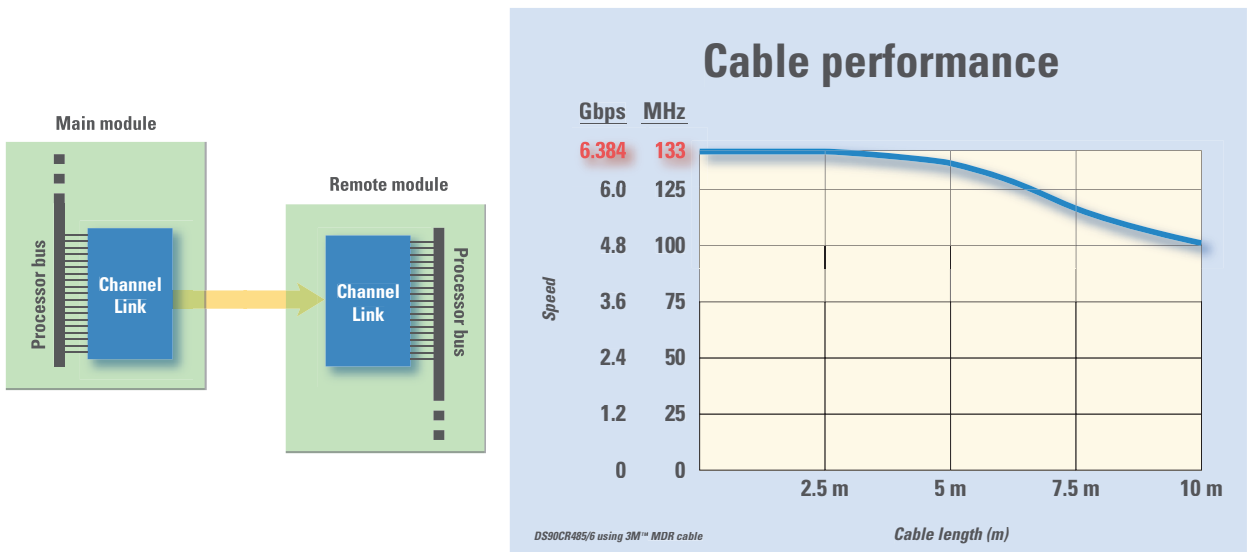
### Supports wide buses

The Channel Link SerDes chipsets act as “virtual ribbon cable” for traditional wide “data+address+control” buses such as control and processor buses. Having no need for channel alignment or synchronization training patterns, Channel Link provides an easy and inexpensive solution for moving wide buses from module to module over cable or backplane.



### Virtual ribbon cable

Channel Link extends wide buses up to 133 MHz over several meters of SCSI-type cable, making data, control, and clock signals available real time to a remote module. No additional protocol or formatting is required.

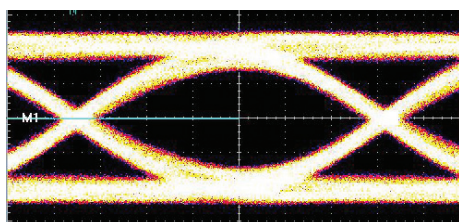
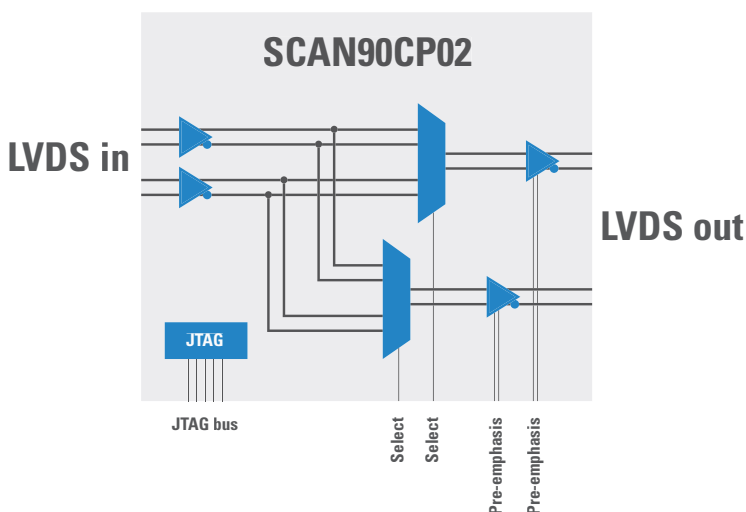


# Using buffers with FPGAs

World's first LVDS buffer with pre-emphasis

## SCAN90CP02

1.5 Gbps 2x2 Crosspoint with pre-emphasis and JTAG



Eye pattern after 10 m of CAT5 cable.

### Product description

The SCAN90CP02 is a 1.5 Gbps 2 x 2 LVDS crosspoint switch with programmable pre-emphasis to drive lossy cables and backplanes. The pre-emphasis of each output is individually pin configurable to one of four levels (off, low, medium, and high) optimizing performance over a variety of interconnects.

### Features

- 1.5 Gbps pre channel operation
- Individually configurable off/low/med/high pre-emphasis outputs
- Non-blocking architecture
- Very low jitter
- IEEE 1149.1 “JTAG” and IEEE 1149.6 “AC-EXTTEST” compliant
- Low 70 mA typical power consumption
- Industrial -40° to +85°C temperature range
- Single 3.3V supply
- Tiny 5 x 5 mm 28-lead LLP® package

### Pricing (1k+ quantities)

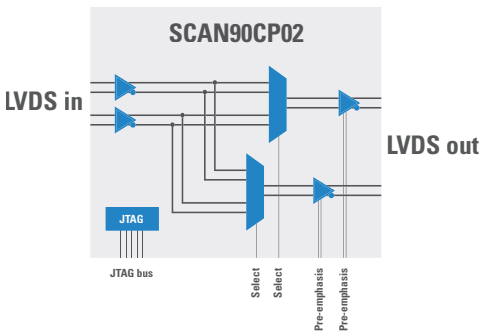
- SCAN90CP02 \$4.95

## Other selected LVDS buffers

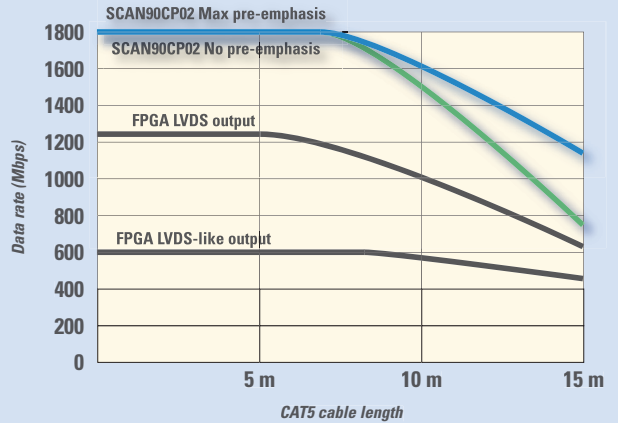
Part number	Function	Speed	Input compatibility	Package(s)
DS92001	Single Bus LVDS buffer	400 Mbps	LVDS/LVPECL	SOIC-8, LLP-8
DS90LV001	Single LVDS buffer	800 Mbps	LVDS/LVPECL	SOIC-8, LLP-8
DS90CK16	1:6 clock distributor	125 MHz	LVDS	TSSOP-24
DS90LV110	1:10 clock/data distributor	800 Mbps	LVDS	TSSOP-28
DS90CP22	2 x 2 Crosspoint switch	800 Mbps	LVDS/LVPECL	SOIC-16
DS90CP04	4 x 4 Crosspoint switch	2.5 Gbps	LVDS/LVPECL	LLP-32

### Boost FPGA LVDS signals

The SCAN90CP02 can be used to boost speed and distance over cables and backplanes. Even without pre-emphasis performance is impressive. With pre-emphasis, LVDS signal quality and reach are improved even further.

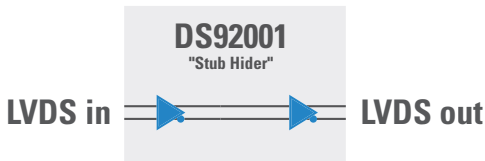


### Speed vs. CAT5 cable length

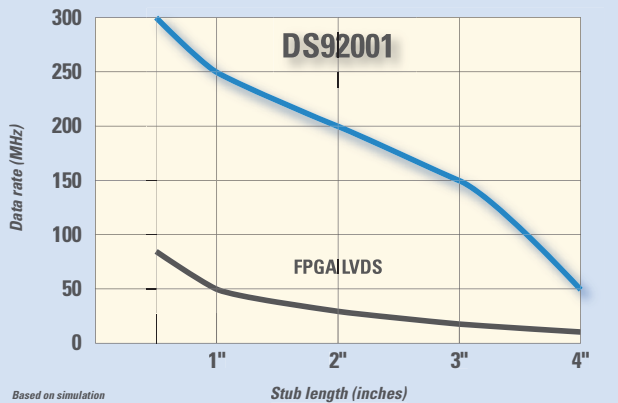


### Reduce stubs

The electrical distance or “stub” between LVDS I/O and the backplane cause reflections in multidrop and multipoint backplanes, robbing performance. It’s difficult, however, to avoid large stubs with large FPGA packages. Using an LVDS-LVDS buffer such as the DS92001 or DS90LV001 reduces these stubs, improving signal quality and maximizing performance.

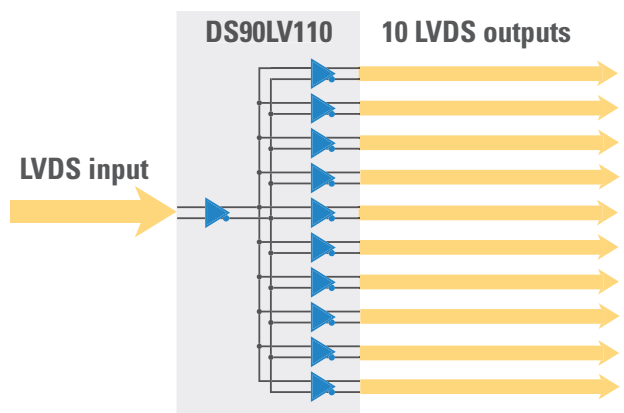


### Speed vs. stub length



### Save FPGA I/O resources

FPGA LVDS I/O resources are too valuable to waste on duplicate signals. The DS90LV110 makes up to 10 copies of your FPGA LVDS clock or data signals and distributes the high quality signals to multiple destinations.



## For more information

For more information on LVDS products, applications, samples, etc please visit:

[lvds.national.com](http://lvds.national.com)

For your nearest distributor, visit:

[www.national.com/contacts](http://www.national.com/contacts)



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