

MB90420/425(A)

F2MC-16LX FAMILY
MICROCONTROLLERS

HARDWARE MANUAL
(ABSTRACTS)

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Chapter 1 General

The MB90420/5(A) series are members of the F²MC-16LX microcontroller family.

- 1.1 Product Overview
- 1.2 Features
- 1.3 Block Diagram
- 1.4 Package Dimensions
- 1.5 Pin Assignments
- 1.6 Pin Descriptions

1.1 Product Overview

Table 1-1-1 gives an overview of the MB90420/5(A) series.

◆ Product Lineup

Table 1-1-1 Overview of MB90420/5(A) Series

Features	MB90V420A	MB90F428	MB90F428A	MB90427	MB90427A	MB90428	MB90428A
Lineup	EVA product	Flash product		Mask ROM product			
CPU	F ² MC-16LX CPU						
System clock	On-chip PLL clock multiplication (x1, x2, x3, x4, 1/2 when PLL stops) Min. instruction execution time 62.5 ns (quadrupled at original oscillation of 4 MHz)						
ROM/Flash memory	External	128-KB boot block flash memory with hard-wired reset vector		64-KB mask ROM		128-KB mask ROM	
RAM	6 KB	6 KB		4 KB		6 KB	
CAN Interface	2 CH		1 CH				
Low voltage detection reset	Available	Not available	Available	Not available	Available	Not available	Available
Package	PGA-256		QFP100				

1.2 Features

Table 1-2-1 lists the features of the MB90420/5(A) series.

◆ Features

Table 1-2-1 Features of MB90420/5(A) Series

Function	Feature
UART (1 CH)	Full-duplex double buffer Asynchronous/synchronous transfer (with start/stop bit) Asynchronous: 4808, 5208, 9615, 10417, 19230, 38460, 62500, 500000 bps Synchronous: 500 Kbps, 1 Mbps, 2 Mbps (when fcp = 16 MHz)
Serial I/O	Transfer from MSB or LSB Synchronous transfer of internal and external clocks Clock synchronization at positive and negative edges Baud rate: 31.25 Kbps, 62.5 Kbps, 125 Kbps, 500 Kbps, 1 Mbps (when fcp = 16 MHz)
A/D Converter	10-bit or 8-bit resolution x 8 CH (input multiplex) Conversion time: 6.13 μ s max. (when fcp = 16 MHz)
16-bit reload timer (1 CH)	16-bit reload timer operation (selectable between toggle output and one-shot output) Can select event count function
Clock timer	Operates directly on oscillation clock Can correct oscillation deviation Read/write second/minute/hour register Single interrupt
16-bit input capture (4 CH)	Detects rising edge, falling edge, or both edges 16-bit capture register x 4 Latches counter value of 16-bit free-run timer when edge of pin input detected and causes interrupt request
16-bit PPG (3 CH)	Output pin x 3 Operating clock frequency: fcp, fcp/2 ² , fcp/2 ⁴ , fcp/2 ⁶
CAN Interface* ¹	Conforms to Parts A and B of CAN specification version 2.0 Automatic resending at error Automatic transmission in response to remote frame Supports 16 data and ID sequenced buffers and multiple messages Flexible construction of acceptance filter All bit compares/all bit masks/two partial bit masks supported up to 1 Mbps

*The CAN interface is available on two channels for the MB90420(A) series and on one channel for the MB90425(A) series.

Table 1-2-1 Features of MB90420/5(A) Series (Cont.)

Function	Feature
Stepping motor controller (4 CH)	High current output to each channel x 4 Synchronized 8/10-bit PWM for each channel x 2
External interrupt (8 CH)	8 channels independent Interrupt cause selectable between Low to High transition (edge) and High to Low transition (edge) and between Low and High levels
Sound generator	8-bit PWM signal mixed with tone frequency from 8-bit reload counter PWM frequency: 62.5, 31.2, 15.6, 7.8 kHz (when f _{cp} = 16 MHz) Tone frequency: PWM frequency ÷ 2 ÷ (reload value + 1)
LCD Controller/driver (1 CH)	Segment driver and common driver that can drive LCD directly
Low voltage detection reset ^{*1}	Automatic reset when low voltage detected
I/O Port	Push-pull output and Schmitt trigger input Programmable as input/output or peripheral signal in bits
Flash memory	Supports automatic programming, Embedded Algorithm ^{TM1-2} , program, erase, pause, and restart commands Flag indicating completion of algorithm Hard-wired reset vectors used to indicate fixed boot sectors in flash memory Minato Electronics flash writer Boot block configuration Block erasing Block protection by external programming voltage

*1: The low voltage detection reset is available only for the MB90420A/5A, but not for the MB90420/5 series.

*2: Embedded Algorithm is a registered trademark of Advanced Micro Devices Inc.

1.3 Block Diagram

Figure 1.3.1 shows a block diagram of the MB90420/5(A) series.

◆ Block Diagram*

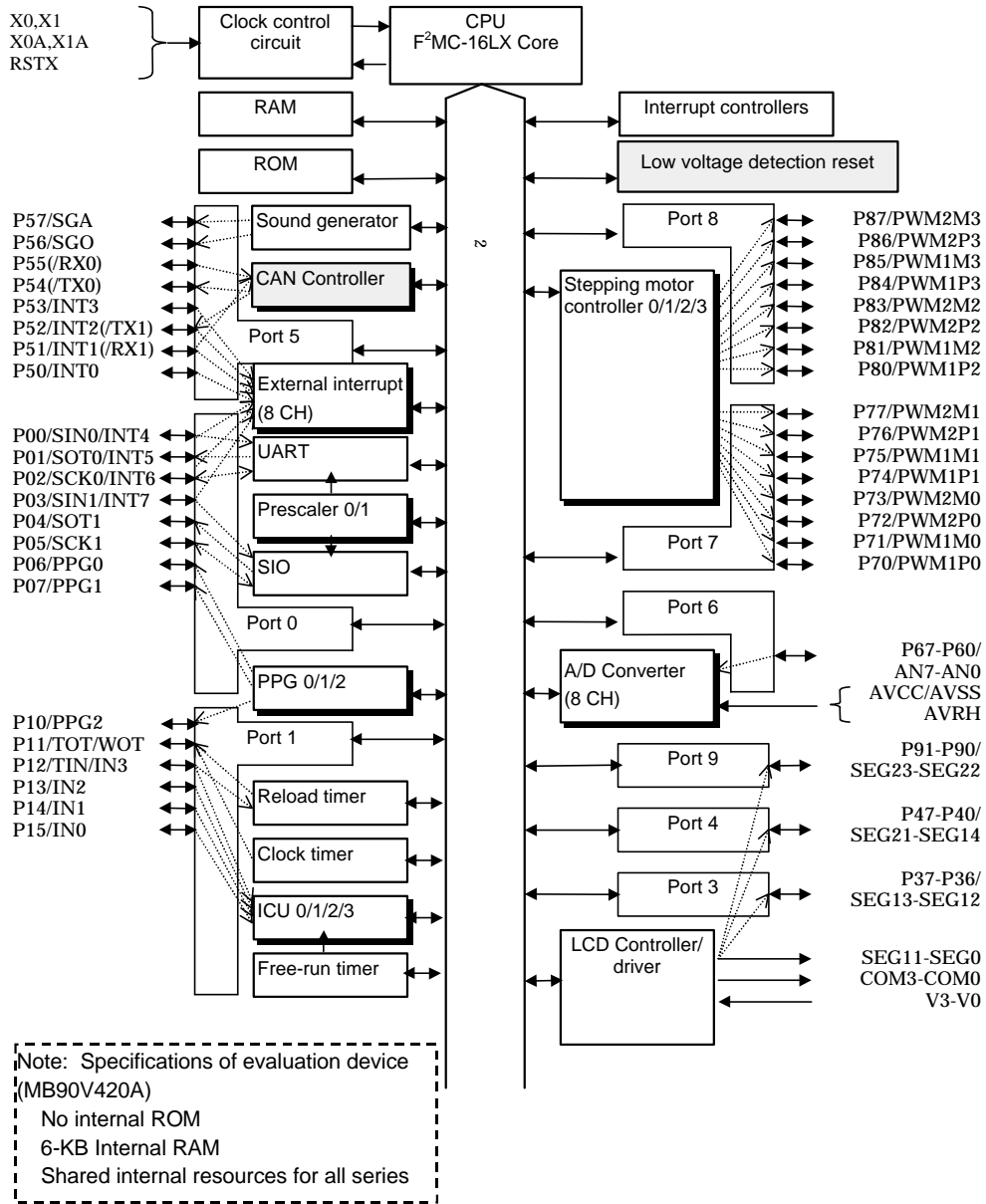


Fig. 1.3.1 Block Diagram

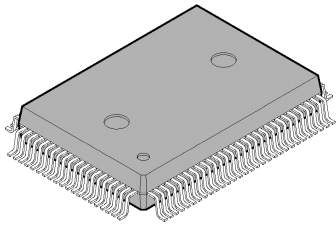
1.4 Package Dimensions

Figure 1.4.1 shows the package dimensions of the MB90420/5(A) series.

◆ Package Dimensions

FPT-100P-M06

EIAJ code: *QFP100-P-1420-4

 <p>100-pin Plastic QFP</p>	Lead pitch	0.65 mm
	Package width x length	14 x 20 mm
	Lead shape	Gull wing
	Sealing	Plastic mold
	Length of pin flat	0.80 mm

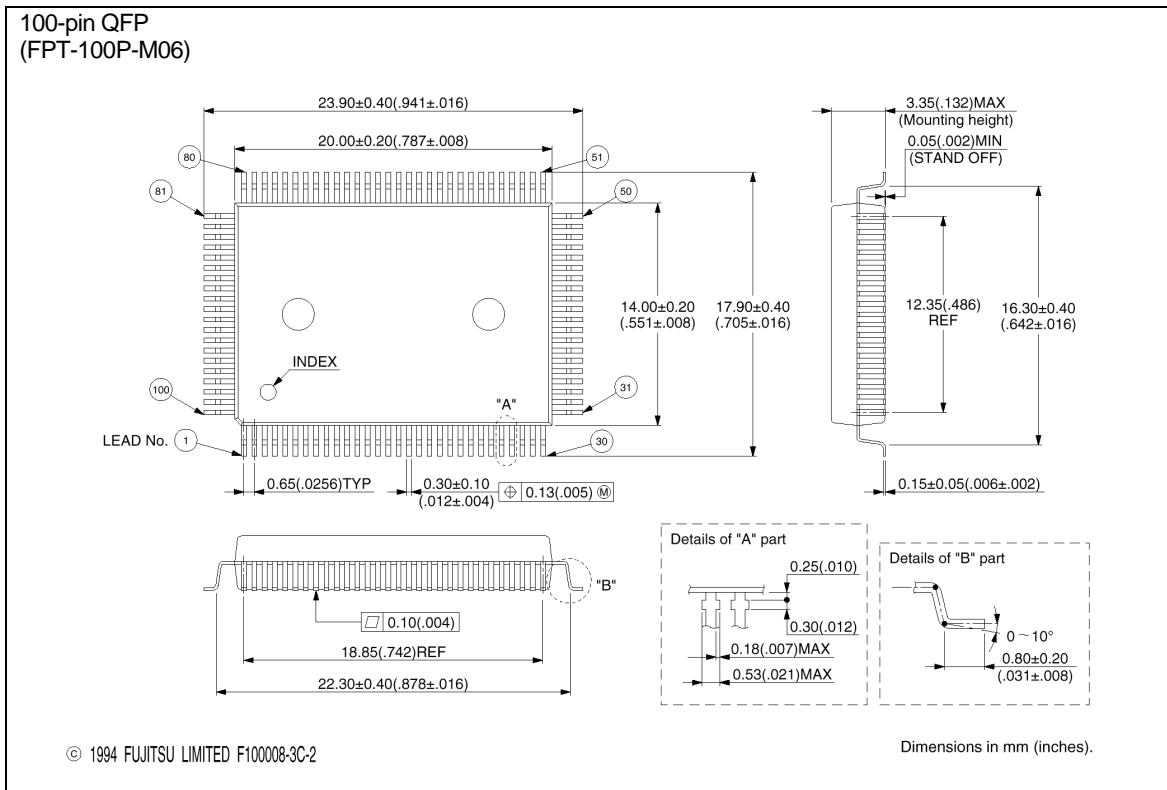


Fig. 1.4.1 Package Dimensions

1.5 Pin Assignments

Figure 1.5.1 shows the pin assignments of the MB90420/5(A) series.

◆ Pin Assignments

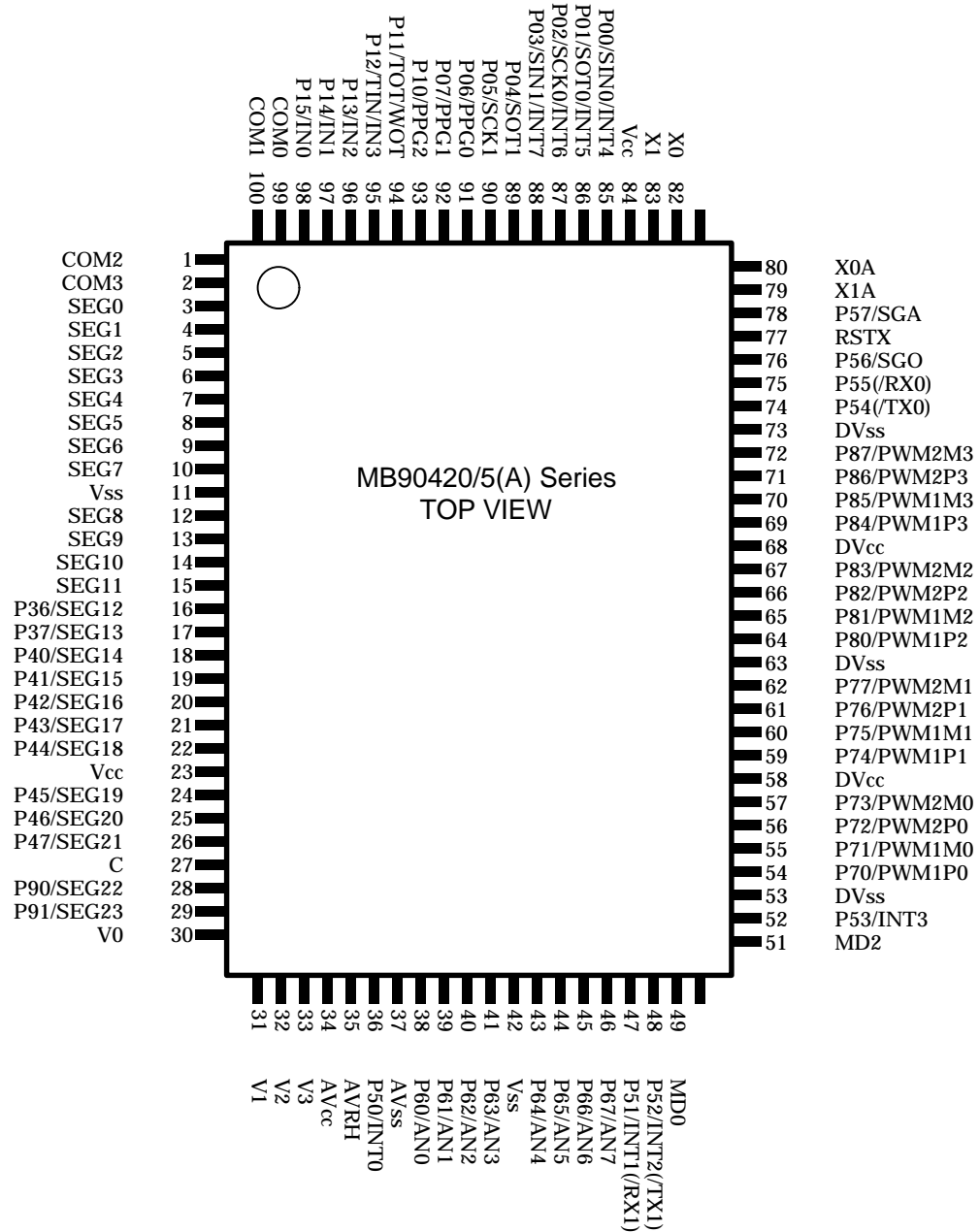


Fig. 1.5.1 Pin Assignments

1.6 Pin Descriptions

Table 1-6-1 gives the pin descriptions of the MB90420/5(A) series.

◆ Pin Descriptions

Table 1-6-1 Pin Descriptions

Pin No.	Pin Name	Function
82	X0	High-speed oscillation input pin
83	X1	High-speed oscillation output pin
80	X0A	Low-speed oscillation input pin
79	X1A	Low-speed oscillation output pin
77	RSTX	Reset input pin
85	P00	General-purpose I/O port
	SIN0	Serial data input pin for UARTCH 0
	INT4	INT4 External interrupt input pin
86	P01	General-purpose I/O port
	SOT0	Serial data output pin for UART CH 0
	INT5	INT5 External interrupt input pin
87	P02	General-purpose I/O port
	SCK0	Serial clock input/output pin for UART CH 0
	INT6	INT6 External input pin
88	P03	General-purpose I/O port
	SIN1	SIN Input pin for serial I/O
	INT7	INT7 External input pin
89	P04	General-purpose I/O port
	SOT1	SOT Output pin for serial I/O
90	P05	General-purpose I/O port
	SCK1	SCK Input/output pin for serial I/O
91 to 93	P06 to P07,P10	General-purpose I/O ports
	PPG0 to PPG2	Output pins for PPG CH 0 to CH 2
94	P11	General-purpose I/O port
	TOT	TOT Output pin for 16-bit reload timer
	WOT	WOT Output pin for clock timer
95	P12	General-purpose I/O port
	TIN	TIN Input pin for 16-bit reload timer
	IN3	Trigger input pin for input capture CH 3
96 to 98	P13 to P15	General-purpose I/O ports
	IN2 to IN0	Trigger input pins for input capture CH 0 to CH 2

Table 1-6-1 Pin Descriptions (Cont.)

Pin No.	Pin Name	Function
99 to 100, 1 to 2	COM0 to COM3	Common output pins for LCD controller/driver
3 to 10, 12 to 15	SEG0 to SEG11	LCD Segment output pins for LCD controller/driver
16 to 17	P36 to P37	General-purpose I/O ports
	SEG12 to SEG13	LCD Segment output pins for LCD controller/driver
18 to 22, 24 to 26	P40 to P47	General-purpose I/O ports
	SEG14 to SEG21	LCD Segment output pins for LCD controller/driver
28 to 29	P90 to P91	General-purpose I/O ports
	SEG22 to SEG23	LCD Segment output pins for LCD controller/driver
36	P50	General-purpose I/O port
	INT0	INT0 External interrupt input pin
38 to 41, 43 to 46	P60 to P67	General-purpose I/O ports
	AN0 to AN7	Input pins for A/D converter
47	P51	General-purpose I/O port
	INT1	INT1 External interrupt input pin
	(RX1)	RX Input pin for CAN interface 1
48	P52	General-purpose I/O port
	INT2	INT2 External interrupt input pin
	(TX1)	TX Output pin for CAN interface 1
52	P53	General-purpose I/O port
	INT3	INT3 External interrupt input pin
54 to 57	P70 to P73	General-purpose I/O ports
	PWM1P0 PWM1M0 PWM2P0 PWM2M0	Output pins for stepping motor controller CH 0
59 to 62	P74 to P77	General-purpose I/O ports
	PWM1P1 PWM1M1 PWM2P1 PWM2M1	Output pins for stepping motor controller CH 1
64 to 67	P80 to P83	General-purpose I/O ports
	PWM1P2 PWM1M2 PWM2P2 PWM2M2	Output pins for stepping motor controller CH 2
69 to 72	P84 to P87	General-purpose I/O ports
	PWM1P3 PWM1M3 PWM2P3 PWM2M3	Output pins for stepping motor controller CH 3

Table 1-6-1 Pin Descriptions (Cont.)

Pin No.	Pin Name	Function
74	P54	General-purpose I/O port
	(TX0)	TX Output pin for CAN interface 0
75	P55	General-purpose I/O port
	(RX0)	RX Input pin for CAN interface 0
76	P56	General-purpose I/O port
	SGO	SGO Output pin for sound generator
78	P57	General-purpose I/O port
	SGA	SGA Output pin for sound generator
30 to 33	V0 to V3	Reference voltage pins for LCD controller/driver
58 68	DVCC	Power input pins for high current output buffer (pin nos. 54 to 72)
53 63 73	DVSS	GND Power pins for high current output buffer (pin nos. 54 to 72)
34	AVCC	Power input pin for A/D converter
37	AVSS	GND Power pin for A/D converter
35	AVR	Vref+ input pin for A/D converter; Vref- fixed to AVSS
49 50	MD0 MD1	Test mode input pins; should be connected to VCC
51	MD2	Test mode input pin; should be connected to VSS
27	C	Pin for external capacitor; 0.1- μ F capacitor should be connected between this pin and VSS
23 84	VCC	Power input pins
11 42 81	VSS	GND Power pins