

MB90565 SERIES

Electric Specification Table

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rated Value		Units	Remarks
		Min.	Max.		
Power supply voltage	V _{CC}	V _{SS} -0.3	V _{SS} +4.0	V	
	AV _{CC}	V _{SS} -0.3	V _{SS} +4.0	V	V _{CC} ≥ AV _{CC} *1
	AVR	V _{SS} -0.3	V _{SS} +4.0	V	AV _{CC} ≥ AVR ≥ 0 V
Input voltage	V _I	V _{SS} -0.3	V _{SS} +4.0	V	*2
Output voltage	V _O	V _{SS} -0.3	V _{SS} +4.0	V	*2
"L" level max. output current	I _{OL}	—	15	mA	*3
"L" level avg. output current	I _{OLAV}	—	4	mA	Average value (Operating current × Operating rate)
"L" level max. overall output current	ΣI _{OL}	—	100	mA	
"L" level avg. overall output current	ΣI _{OLAV}	—	50	mA	Average value (Operating current × Operating rate)
"H" level max. output current	I _{OH}	—	-15	mA	*3
"H" level avg. output current	I _{OHAV}	—	-4	mA	Average value (Operating current × Operating rate)
"H" level max. overall output current	ΣI _{OH}	—	-100	mA	
"H" level avg. overall output current	ΣI _{OHAV}	—	-50	mA	Average value (Operating current × Operating rate)
Power consumption	P _D	—	300	mW	
Operating temperature	T _A	-40	+85	°C	
Storage temperature	T _{STG}	-55	+150	°C	

*1: AV_{CC} should not exceed V_{CC} when turning on the power supply.

*2: V_I and V_O should not exceed V_{CC} +0.3 V.

*3: The maximum output current is standard at the peak value of the corresponding 1 pin.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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2. Recommended Conditions

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Rated Value		Units	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	3.0	3.6	V	Under normal operation (MB90V560)
		2.7	3.6	V	Under normal operation (MB90F568)
		2.7	3.6	V	Under normal operation (MB90567/568)
	V_{CC}	2.5	3.6	V	Maintains status of stop operation
Input H voltage	V_{IH}	$0.7 V_{CC}$	$V_{CC} + 0.3$	V	CMOS input pin
	V_{IHS}	$0.8 V_{CC}$	$V_{CC} + 0.3$	V	CMOS hysteresis input pin
	V_{IHM}	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	MD pin input
Input L voltage	V_{IL}	$V_{SS} - 0.3$	$0.3 V_{CC}$	V	CMOS pin input
	V_{ILS}	$V_{SS} - 0.3$	$0.2 V_{CC}$	V	CMOS hysteresis input pin
	V_{ILM}	$V_{SS} - 0.3$	$V_{SS} + 0.3$	V	MD pin input
Operating temperature	T_A	-40	+85	°C	

3. DC Characteristics

(T_A = -40° to +85°C, V_{CC} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Test Condition	Rated Value			Units	Remarks
				Min.	Typ.	Max.		
Output H voltage	V _{OH}	All output pins	V _{CC} = 3.0 V, I _{OH} = -2.0 mA	V _{CC} -0.5	V _{CC} -0.3	—	V	
Output L voltage	V _{OL}	All output pins	V _{CC} = 3.0 V, I _{OL} = 2.0 mA	—	0.2	0.4	V	
Input leak current	I _{IL}	All output pins	V _{CC} = 3.0 V, V _{SS} < V _I < V _{CC}	-5	-1	5	μA	
Power supply current *	I _{CC}	V _{CC}	V _{CC} = 3.3 V, Internal frequency: 8 MHz, At normal operating	—	14	22	mA	MB90567/568
			V _{CC} = 3.3 V, Internal frequency: 16 MHz, At normal operating	—	27	40	mA	MB90567/568
			V _{CC} = 3.3 V, Internal frequency: 8 MHz, At A/D operatin	—	18	27	mA	MB90567/568
			V _{CC} = 3.3 V, Internal frequency: 16 MHz, At normal operating	—	32	45	mA	MB90567/568
			V _{CC} = 3.3 V, Internal frequency: 8 MHz, At normal operating	—	18	28	mA	MB90F568
			V _{CC} = 3.3 V, Internal frequency: 16 MHz, At normal operatin	—	36	45	mA	MB90F568
			V _{CC} = 3.3 V, Internal frequency: 8 MHz, At A/D operatin	—	23	33	mA	MB90F568
			V _{CC} = 3.3 V, Internal frequency: 16 MHz, At A/D operatin	—	41	50	mA	MB90F568
			Flash programming/erase	—	40	50	mA	MB90F568
	I _{CCS}	V _{CC}	V _{CC} = 3.3 V, Internal frequency: 8 MHz, At sleep	—	6	10	mA	MB90567/568 MB90F568* ¹
			V _{CC} = 3.3 V, Internal frequency: 16 MHz, At sleep	—	14	20	mA	MB90567/568 MB90F568* ¹
I _{CCH}			At stop, T _A = 25°C	—	5	20	μA	
Pull-up resistor	R _{UP}	P00 to P07, P10 to P17, RST, MD0, MD1		20	65	200	kΩ	
Pull-down resistor	R _{DOWN}	MD2	—	20	65	200	kΩ	

*: Values are provided when the low-power mode bits (LPM0 and LPM1) are set to '01' at an internal operating frequency of 8 MHz.
 Note: Current values are tentative. They are subject to change without notice according to improvements in the characteristics. The power supply current testing conditions are when using the external clock.

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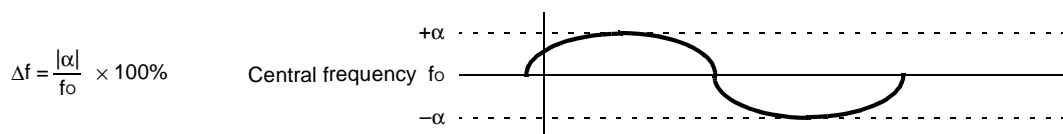
4. AC Characteristics

(1) Clock Timing

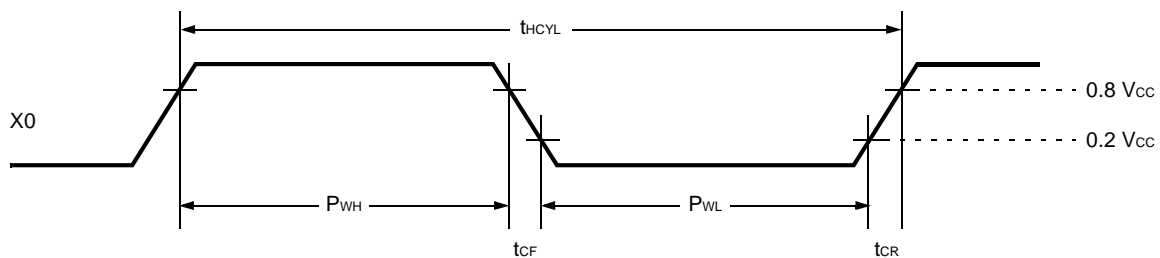
(MB90567/568/F568: $T_A = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS} = 0.0$ V)
 (MB90V560: $T_A = +25^\circ\text{C}$, $V_{CC} = 3.0$ to 3.6 V, $V_{SS} = AV_{SS} = 0.0$ V)

Parameter	Symbol	Pin	Test Condition	Rated Value			Units	Remarks
				Min.	Typ.	Max.		
Clock frequency	f_c	X0, X1	—	3	—	12	MHz	MB90V560
				3	—	16	MHz	MB90567/568 MB90F568
Clock cycle time	t_{HCYL}	X0, X1	—	83.3	—	333	ns	MB90V560
				62.5	—	333	ns	MB90567/568 MB90F568
Frequency varying rate* (At lock)	Δf	—	—	—	5	%		
Input clock pulse width	P_{WH} P_{WL}	X0	—	10	—	ns	Duty ratio is about 30 to 70%.	
Input clock rise and fall time	t_{CR} t_{CF}	X0	—	—	5	ns	At using external clock	
Internal operation clock frequency	f_{CP}	—	—	1.5	—	12	MHz	MB90V560
				1.5	—	16	MHz	MB90567/568 MB90F568
Internal operation clock cycle time	t_{CP}	—	—	83.3	—	666	ns	MB90V560
				62.5	—	666	ns	MB90567/568 MB90F568

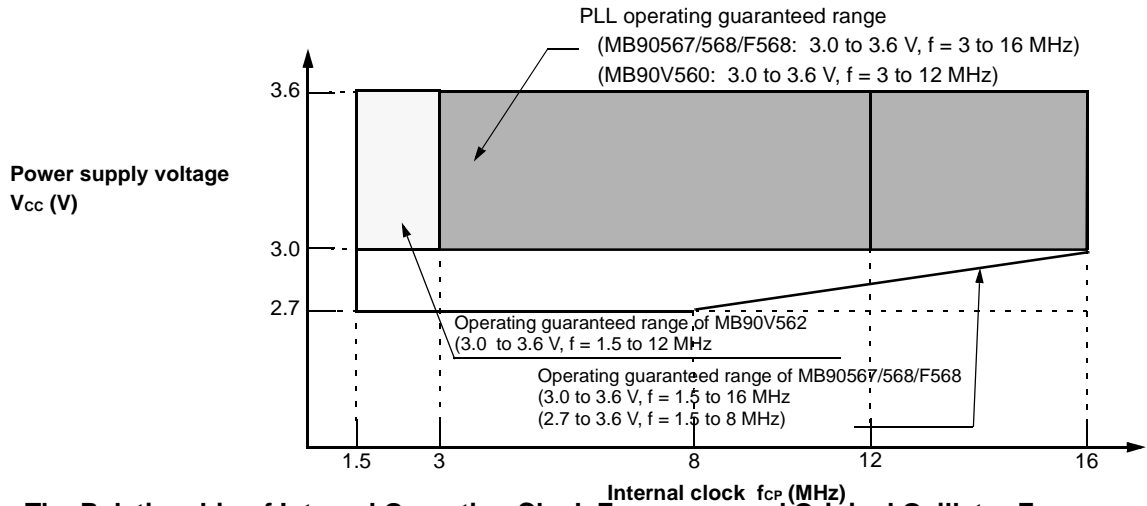
*: Frequency Varying Rate is the maximum variable ratio from the set central frequency when using a multiplied clock.



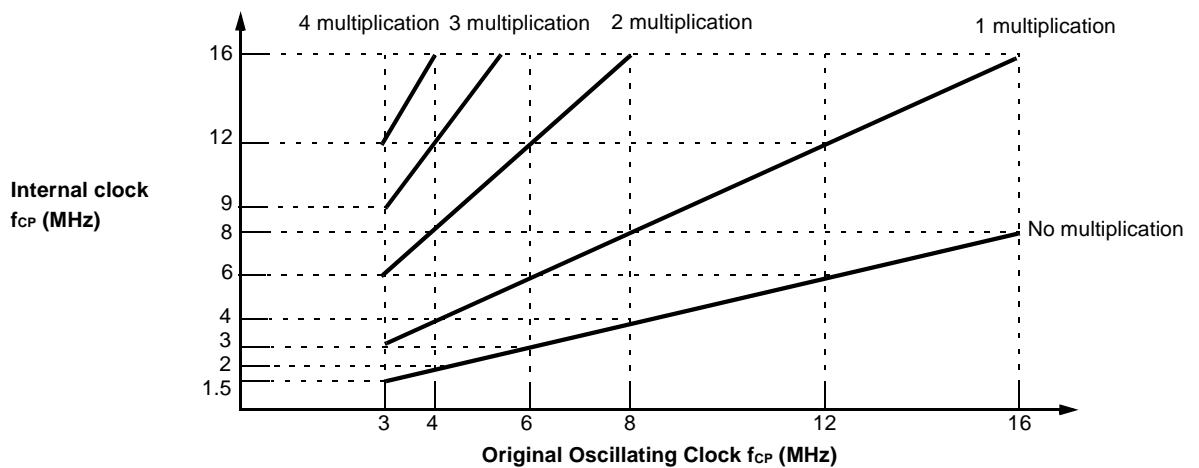
• X0, X1 clock timing



• PLL operating guaranteed range



The Relationship of Internal Operating Clock Frequency and Original Oscillator Frequency

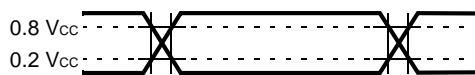


The Relationship of Original Oscillator Frequency and Internal Operation Clock Frequency

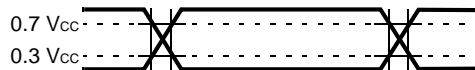
AC characteristics are set to the measured reference voltage values below.

• Input signal waveform

Hysteresis Input Pin

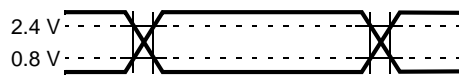


Other than Hysteresis Input/MD Input Pin



• Output signal waveform

Output Pin

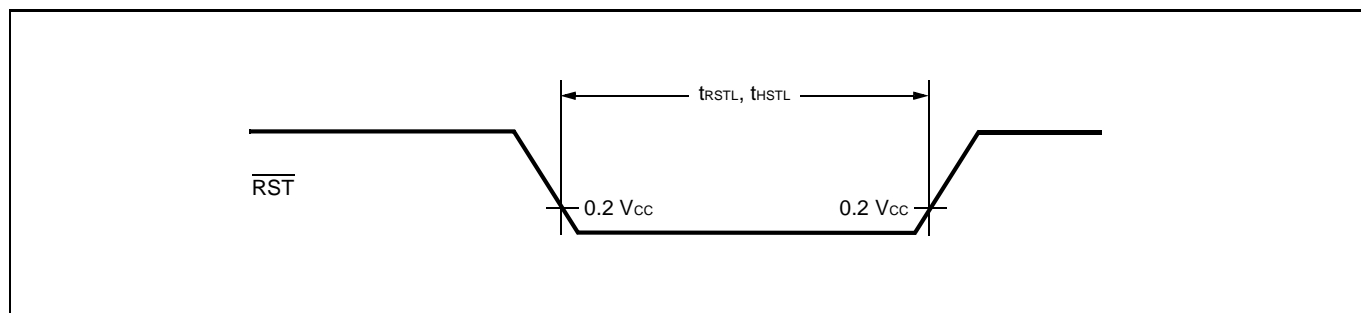


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(2) Reset

($T_A = -40^\circ$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.6 V , $V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	\overline{RST}	—	4 t_{CP}	—	ns	



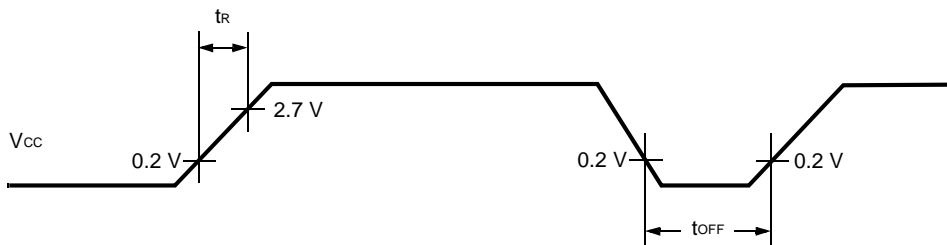
(3) Power On Reset

($T_A = -40^\circ$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.6 V , $V_{SS} = AV_{SS} = 0.0\text{ V}$)

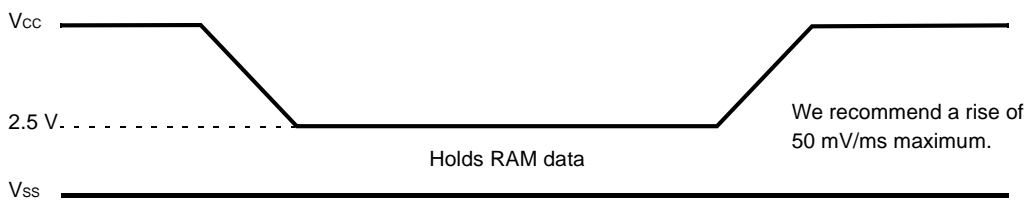
Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min.	Max.		
Power rise time*	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		4	—	ms	As operation is repeated

*: $V_{CC} < 0.2\text{ V}$ must be given before power-on.

- Notes: 1. The above specifications are numeric values used to trigger a power-on reset.
 2. The device contains registers that are initialized only by a power-on reset. To initialize these registers, turn the power on according to the above specifications.



If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 mV/sec, you can operate while using the PLL clock.



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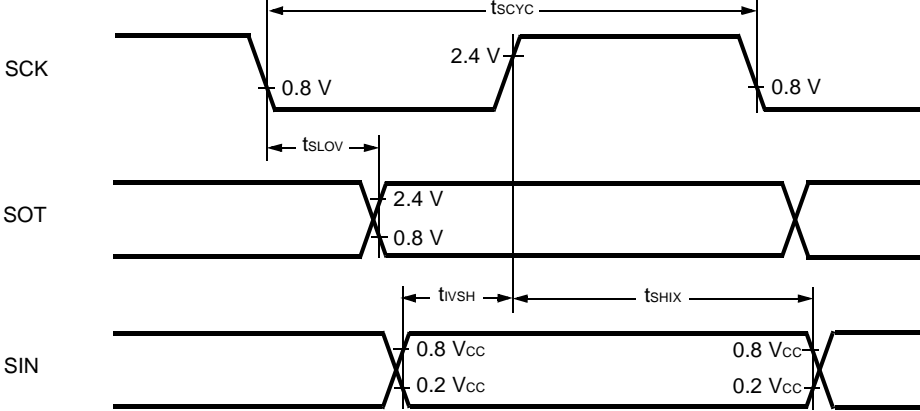
(4) UART 0, 1

(T_A = -40° to +85°C, V_{CC} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

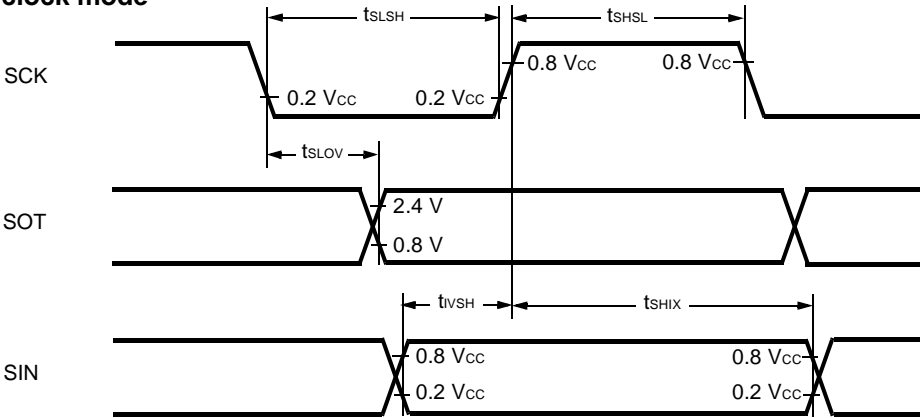
Parameter	Symbol	Pin Symbol	Test Condition	Rated Value		Units	Remarks
				Min.	Max.		
Serial clock cycle time	t _{SCYC}	SCK0 to SCK1	Internal shift clock mode output pins are C _L = 80 pF + 1 TTL.	8 t _{CP}	—	ns	
SCK ↓ ⇒ SOT delay time	t _{SLOV}	SCK0 to SCK1, SOT0 to SOT1		-80	80	ns	
Valid SIN ⇒ SCK ↑	t _{IVSH}	SCK0 to SCK1, SIN0 to SIN1		100	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t _{SHIX}	SCK0 to SCK1, SIN0 to SIN1		60	—	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0 to SCK1	External shift clock mode output pins are C _L = 80 pF + 1 TTL.	4 t _{CP}	—	ns	
Serial clock "L" pulse width	t _{LSLH}	SCK0 to SCK1		4 t _{CP}	—	ns	
SCK ↓ ⇒ SOT delay time	t _{SLOV}	SCK0 to SCK1, SOT0 to SOT1		—	150	ns	
Valid SIN ⇒ SCK ↑	t _{IVSH}	SCK0 to SCK1, SIN0 to SIN1		60	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t _{SHIX}	SCK0 to SCK1, SIN0 to SIN1		60	—	ns	

- Notes: 1. AC characteristic in CLK synchronized mode.
 2. C_L is load capacity value of pins when testing.
 3. t_{CP} is the machine cycle (Unit: ns).

• Internal shift clock mode



• External shift clock mode

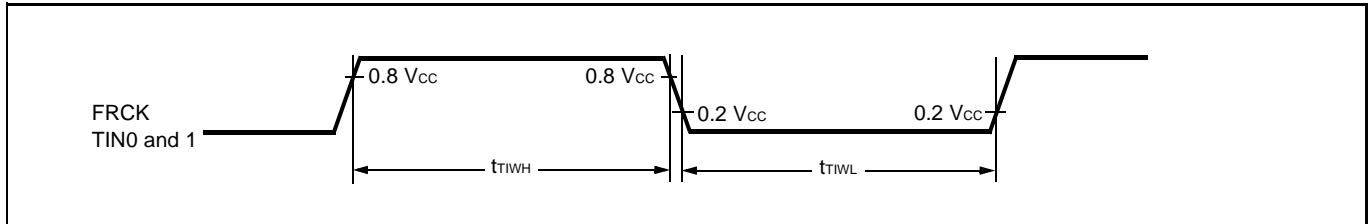


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(5) Timer Input Timing

($T_A = -40^\circ$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.6 V , $V_{SS} = AV_{SS} = 0.0\text{ V}$)

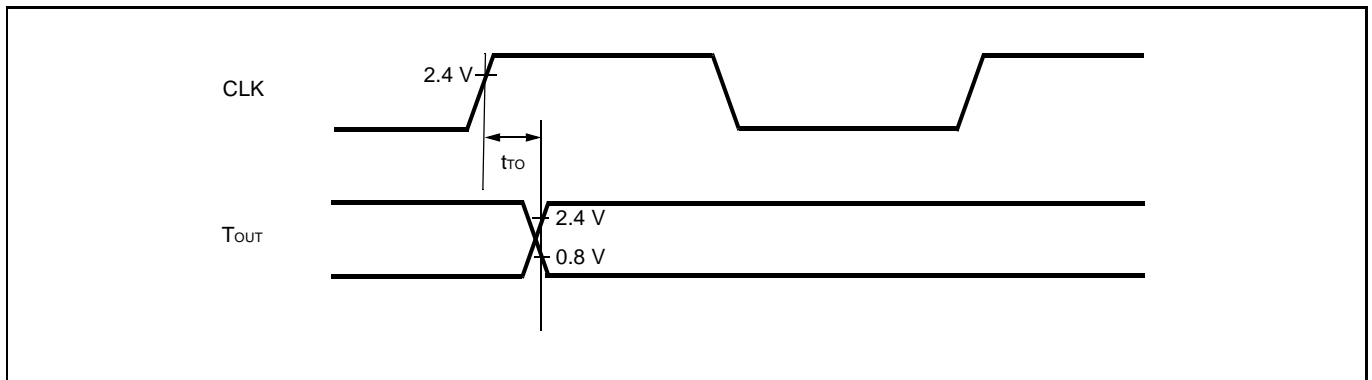
Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min.	Max.		
Input pulse width	t_{RIWH} t_{RIWL}	FRCK TIN0 to TIN1	—	4 t_{CP}	—	ns	



(6) Timer Output Timing

($T_A = -40^\circ$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.6 V , $V_{SS} = AV_{SS} = 0.0\text{ V}$)

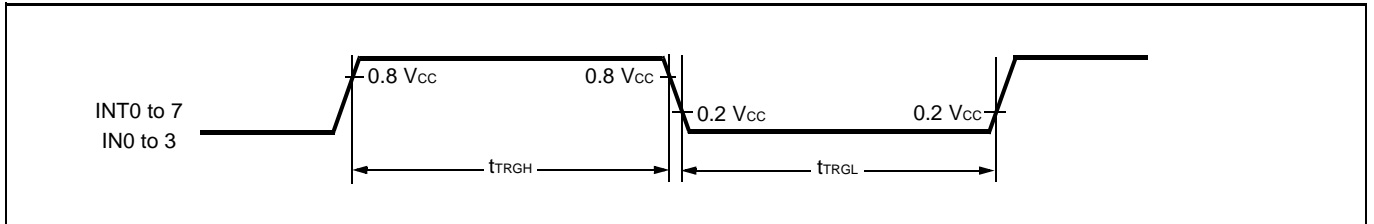
Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min.	Max.		
CLK \uparrow \Rightarrow T _{OUT} change time	t_{RO}	RTO 0 to RTO5 PPG0 to PPG5 TO0 to TO1	—	30	—	ns	



(7) Trigger Input Timing

($T_A = -40^\circ$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.6 V , $V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min.	Max.		
Input pulse width	t_{TRGL}	INT0 to INT7 IN0 to IN3	—	5 t_{CP}	—	ns	



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5. A/D Conversion Unit Electrical Characteristics

(MB90567/568/F568: $T_A = -40^\circ$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq \text{AVR}$, $V_{CC} = \text{AV}_{CC} = 2.7$ to 3.6 V , $V_{SS} = \text{AV}_{SS} = 0.0\text{ V}$)

MB90V560: $T_A = +25^\circ\text{C}$, $3.0\text{ V} \leq \text{AVR}$, $V_{CC} = \text{AV}_{CC} = 3.0$ to 3.6 V , $V_{SS} = \text{AV}_{SS} = 0.0\text{ V}$)

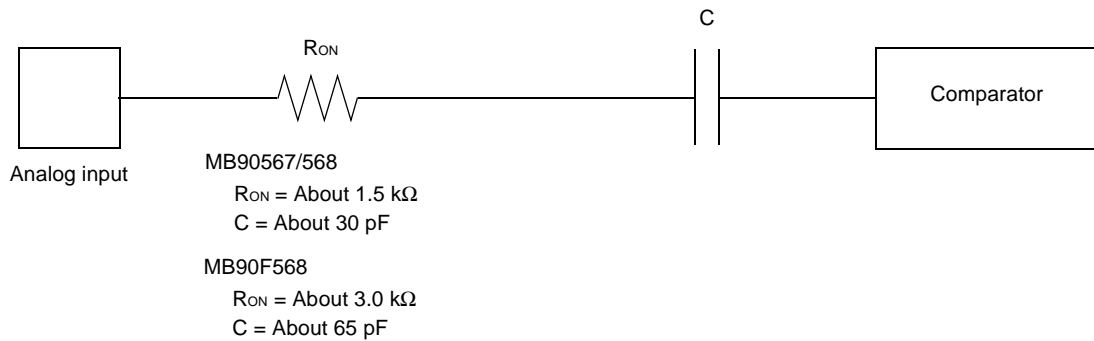
Parameter	Symbol	Pin	Rated Value			Units	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	10	10	bit	
Overall error	—	—	—	—	± 3.0	LSB	
Non-linearity error	—	—	—	—	± 2.5	LSB	
Differential linearity error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} -1.5LSB	AV_{SS} $+0.5$	AV_{SS} $+2.5\text{LSB}$	mV	1LSB = AVR/1024
Full scale transition voltage	V_{FST}	AN0 to AN7	AVR -3.5LSB	AVR -1.5LSB	AVR $+0.5\text{LSB}$	mV	
Conversion time	—	—	—	66 t_{CP}	—	ns	
Sampling time	—	—	—	32 t_{CP}	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	μA	
Analog input voltage	V_{AIN}	AN0 to AN7	0	—	AVR	V	
Reference voltage	—	AVR	2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	1	5	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*1
Reference voltage supply current	I_R	AVR	—	100	200	μA	
	I_{RH}	AVR	—	—	5	μA	*1
Channel differences	—	AN0 to AN7	—	—	4	LSB	

*1: When not operating A/D converter, this is the current ($V_{CC} = \text{AV}_{CC} = \text{AVR} = 3.3\text{ V}$) when the CPU is stopped.

Notes:

- Reference L is fixed at AV_{SS} . The difference is relatively large as the AVR becomes smaller.
- Analog input external circuit output impedance should use the following conditions.
External Circuit Output Impedance $\leq 10\text{ k}\Omega$
- If the external circuit output impedance is too high, there may be insufficient time for sampling of the analog voltage.

• Analog input equivalent circuit diagram



Note: Numeric values herein should be used as a guide.

6. Handling Device

- **Preventing latch-up**

Latch-up may occur in CMOSIC when a voltage higher than V_{CC} or lower than V_{SS} is applied to the input or output pins, or a voltage exceeding the rated value is applied between V_{CC} and V_{SS} . Latch-up may cause a rapid increase in the supply current, sometimes resulting in thermal damage to the device. Therefore, keep the used voltage within the maximum ratings.

When turning the power on and off the analog supply voltage (AV_{CC} , AVR) and analog input should not exceed the digital supply voltage (V_{CC})

- **Voltage supplies should be stabilized.**

A sudden change of the power supply voltage may cause a malfunction even within the guaranteed range of operation of the power supply voltage.

For reference of stabilization, voltage variations are recommended to be restrained so that V_{CC} ripple variations (P-P values) are below 10% of the standard V_{CC} value in commercial frequencies (50 to 60 Hz), and so that transient variation is below 0.1 V/ms in sudden changes during power switchovers.

- **Precautions when turning on the power supply**

Ensure a minimum of 50 μ s (between 0.2 to 2.7 V) for voltage rise times when turning on the power supply to prevent malfunction of the built-in power reduction circuit.

- **Handling of unused input pins**

Leaving unused input pins open may cause a malfunction. Therefore, these pins should be connected to a pull-up or a Pull-down resistor.

- **Handling of N.C. pins**

Always leave N.C. pins (internal connections) open.

- **Handling of A/D converters power supply pins**

Connect power supply pins with $AV_{CC} = V_{CC}$, $AV_{SS} = AVR = V_{SS}$ even when not using the A/D converters.

- **Precautions when using the external clock**

Oscillating stability waiting time is required when resetting from the Power On Reset, Sub-clock Mode and Stop Mode when using the external clock.

- **Order of turning on the power**

Turn off the digital power supply (V_{CC}) after turning off the A/D converter power supplies (AV_{CC} , AVR) and analog input ($AN0$ to $AN7$).

Do not allow the AVR to exceed AV_{CC} when turning the power on and off.

Do not allow the input voltage to exceed AV_{CC} when using the analog input pins as an input port.

PRECAUTIONS WHEN USING MB90F568/567/568 SPECIFICATIONS

The following shows the precautions, specifications and the recommended connections of the MB90F567/567/568 and MB90F562/562.

(1) Changes in specification functions

- 1) The 5 V-3 V regulator was deleted.
The C pin is used as a NC pin.
- 2) The conversion part of the A/D converter was changed from 5 to 3 V.
There are no changes to conversion time and sampling time.
- 3) The withstand voltage of the I/O pin was changed from 5 to 3 V.
- 4) The transfer counter clear function of the UART was added.
This function resets only the UART to its initial state by writing 0 to the UART reset bit.

(2) Precautions on using

When writing on-board, SIN uses P60 (14), SOT uses P61 (15) and SCK uses P40 (60) (Same the MB90F562).

• On-board Writing

This product supports on-board writing. When writing on-board, use the pin settings shown in the table below.

Pin Name	Pin I/O Level	Remarks
MD2	H level	Serial write mode setting
MD1	H level	
MD0	L level	
SIN1	Serial data input	Normally used with P60
SOT1	Serial data output	Normally used with P61
SCK0	Serial clock	Normally used with P40
P00	L level	
P01	H level	When writing PC, L level is input

Notes:

- 1) Settings in Pin I/O Level are when using a writer for YDC made on-board writing. You can write from a PC, but you need a dedicated write program. Contact **Fujitsu's application engineers** for details.

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