

MB90470 Series

Electric Specification Table

■ Electrical Characteristics

1. Absolute Maximum Rating

(V_{SS} = A_{VSS} = 0.0 V)

Parameter	Symbol	Rated Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V _{CC3}	V _{SS} - 0.3	V _{SS} + 4.0	V	
	V _{CC5}	V _{SS} - 0.3	V _{SS} + 7.0	V	
	A _{VCC}	V _{SS} - 0.3	V _{SS} + 4.0	V	*1
	A _{VRH}	V _{SS} - 0.3	V _{SS} + 4.0	V	
Input voltage	V _I	V _{SS} - 0.3	V _{SS} + 4.0	V	*2
		V _{SS} - 0.3	V _{SS} + 7.0	V	*2
Output voltage	V _O	V _{SS} - 0.3	V _{SS} + 4.0	V	*2
		V _{SS} - 0.3	V _{SS} + 7.0	V	*2
"L" level max. output current	I _{OL}	—	10	mA	*3
"L" level avg. output current	I _{OLAV}	—	3	mA	*4
"L" level max. overall output current	ΣI _{OL}	—	60	mA	
"L" level avg. overall output current	ΣI _{OLAV}	—	30	mA	*5
"H" level max. output current	I _{OH}	—	-10	mA	*3
"H" level avg. output current	I _{OHAV}	—	-3	mA	*4
"H" level max. overall output current	ΣI _{OH}	—	-60	mA	
"H" level avg. overall output current	ΣI _{OHAV}	—	-30	mA	*5
Power consumption	P _D	—	200	mW	
Operating temperature	T _A	-40	+85	°C	
Storage temperature	T _{STG}	-55	+150	°C	

*1: A_{VCC}, A_{VRH} should not exceed V_{CC3}.*2: V_I and V_O should not exceed V_{CC} (including V_{CC3}, V_{CC5}) + 0.3 V.

*3: The maximum output current is standard at the peak value of the corresponding 1 pin.

*4: The average output current is defined as the mean of the current passing through the relevant pin for a period of 100 ms max.

*5: The average total output current is defined as the mean of the current passing through all relevant pins for a period of 100 ms max.

Caution: Use outside the absolute maximum ratings (voltage, current, temperature) can damage semiconductor devices. Never allow any condition to exceed the rating.

2. Recommended Conditions

(V_{SS} = A_{VSS} = 0.0 V)

Parameter	Symbol	Rated value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V _{CC3}	1.8	3.6	V	MASK Version
		2.4	3.6	V	Low-voltage FLASH version
		3.13	3.6	V	High-speed FLASH version
	V _{CC5}	1.8	5.5	V	MASK Version
		2.4	5.5	V	Low-voltage FLASH version
		3.13	3.6	V	High-speed FLASH version
	V _{CC3}	1.8	3.6	V	Maintains status of stop operation
	V _{CC5}	1.8	5.5	V	Maintains status of stop operation (MASK version)
		1.8	5.5	V	Maintains status of stop operation (FLASH version)
“H” level input voltage	V _{IH}	0.7 V _{CC}	V _{CC} + 0.3	V	Pins other than V _{HIS} , V _{IHM}
	V _{IHS}	0.8 V _{CC}	V _{CC} + 0.3	V	Hysteresis input pin
	V _{IHM}	V _{CC} – 0.3	V _{CC} + 0.3	V	MD Pin input
“L” level input voltage	V _{IL}	V _{SS} – 0.3	0.3 V _{CC}	V	Pins other than V _{ILS} , V _{ILM}
	V _{ILS}	V _{SS} – 0.3	0.2 V _{CC}	V	Hysteresis input pin
	V _{ILM}	V _{SS} – 0.3	V _{SS} + 0.3	V	MD pin input
Operation temperature	T _A	–40	+85	°C	

*: When using I²C, apply a voltage of 2.7 V min.

Caution: The recommended operating conditions ensure normal operation of semiconductor devices. The standard values for the electrical characteristics are all assured within the recommended operating conditions. Always use semiconductor devices under the recommended operating conditions. If these conditions are exceeded, the reliability may be adversely affected.

Normal operation of semiconductor devices is not assured if any item, condition, and logic not listed in the electrical specifications is used. If you plan to use semiconductor devices under conditions not listed in the electrical specifications, always consult our Sales Department first.

3. DC Specifications

(MASK version: $V_{CC} = 1.8\text{ V to }3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{ to }+85^\circ\text{C}$
 (Low voltage FLASH version: $V_{CC} = 2.4\text{ V to }3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{ to }+85^\circ\text{C}$)
 (High speed FLASH version: $V_{CC} = 3.13\text{ V to }3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{ to }+85^\circ\text{C}$)

Parameter	Symbol	Pin	Test Condition	Rated value			Unit	Remarks						
				Min.	Typ.	Max.								
Output H voltage	V_{OH}	Pins other than P76 and P77	$V_{CC} = 2.7\text{ V}$ $I_{OH} = -1.6\text{ mA}$	V_{CC3} -0.3	—	—	V	*						
			$V_{CC} = 4.5\text{ V}$ $I_{OH} = -4.0\text{ mA}$	V_{CC5} -0.5	—	—	V	When 5 V power used						
Output L voltage	V_{OL}	All output pin	$V_{CC} = 2.7\text{ V}$ $I_{OL} = 2.0\text{ mA}$	—	—	0.4	V							
			$V_{CC} = 4.5\text{ V}$ $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	When 5 V power used						
Input leak current	I_{IL}	Pins other than P76 and P77	$V_{CC} = 3.3\text{ V}$ $V_{SS} < V_I < V_{CC}$	-10	—	10	μA							
Pull-up resistor	RPULL	—	$V_{CC} = 3.0\text{ V}$, and $T_A = +25^\circ$	20	65	200	$\text{k}\Omega$							
Open drain output current	I_{leak}	P40 to P47, P70 to P77	—	—	0.1	10	μA							
Power supply current	I_{CC}	—	$V_{CC} = 3.3\text{ V}$, and internal operation at 20 MHz, and normal operation	—	40	55	mA	MASK version (Target is TBD.)						
				—	45	60	mA	MASK version (Target is TBD.) (A/D operation)						
				—	51	66	mA	FLASH version						
				—	56	71.5	mA	FLASH version •A/D operation•						
	I_{CCS}	—	$V_{CC} = 3.3\text{ V}$, and internal operation at 20 MHz, and sleep mode	—	18	33	mA							
				I_{CCL}	—	$V_{CC} = 3.3\text{ V}$, and external operation at 32 kHz, and internal operation at 8 kHz, and sub-operation ($T_A = 25^\circ\text{C}$)	—	16	140	μA				
							I_{CCT}	—	$V_{CC} = 3.3\text{ V}$, and external operation at 32 kHz, and internal operation at 8 kHz, and watch operation ($T_A = 25^\circ\text{C}$)	—	10	40	μA	MASK version (Target is TBD.)
										—	15	40	μA	FLASH version
I_{CCH}	—	$T_A = +25^\circ\text{C}$, and operation stopped, and $V_{CC} = 3.3\text{ V}$	—	0.1	20	μA	MASK version (Target is TBD.)							
			—	0.2	40	μA	FLASH version							
Input capacity	C_{IN}	Pins other than AV _{CC} , AV _{SS} , V _{CC} , V _{SS}	—	—	10	80	pF							

- *: P40 to P47 and P70 to P75 are N-ch open-drain pins with control, and are normally used as CMOS.
- *: P76 and P77 are N-ch open-drain pins.
- *: $V_{cc} = V_{cc3} = V_{cc5}$
- *: When a dual power supply is used, P20 to P27, P30 to P37, P40 to P47, and P70 to P77 are 5-V pins; other pins are 3-V input pins.

4. AC Specifications

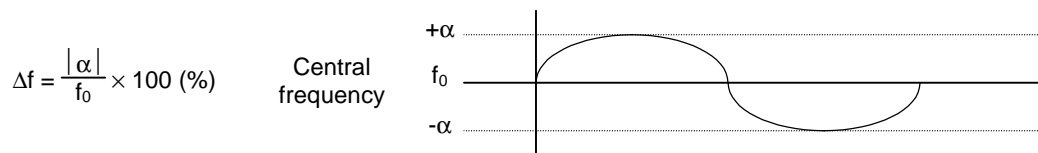
(1) Clock timing specifications

(V_{SS} = 0.0 V, T_A = -40° to +85°C)

Parameter	Symbol	Pin	Test condition	Rated value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F _{CH}	X0, X1	—	3	—	40	MHz	*3
	F _{CL}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t _C	X0, X1		25	—	333	ns	*3
	t _{CL}	X0A, X1A		—	30.5	—	μs	
Input clock pulse width	P _{WH} P _{WL}	X0		5	—	—	ns	*2
	P _{WLH} P _{WLL}	X0A		—	15.2	—	μs	*2
Input clock rise, fall time	t _{cr} t _{cf}	X0		—	—	5	ns	External clock used
Internal operation clock frequency	f _{CP}	—		1.5	—	20	MHz	*3
	f _{CPL}	—		—	8.192	—	kHz	
Internal operation clock cycle time	t _{CP}	—		50.0	—	666	ns	*3
	t _{CPL}	—		—	122.1	—	μs	
Frequency varying time	Δf	—		—	—	5	%	During lock*1

*1: Frequency varying rate is the maximum variable ratio from the set central frequency when PLL used multiplication is locked.

*2: V_{CC} = V_{CC3} = V_{CC5}

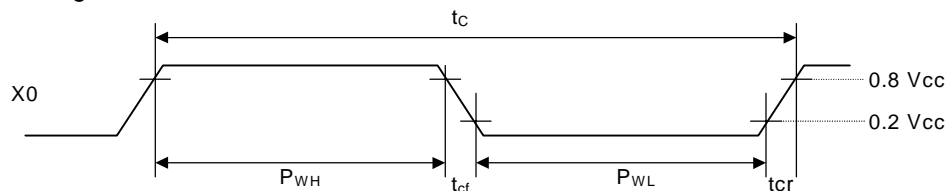


The PLL frequency varying rate fluctuates at a certain cycle (about CLK × (1 CYC to 50 CYCs)) from the specified frequency. So, the worst value does not necessarily appear continuously (There is almost no error with long-cycle pulses).

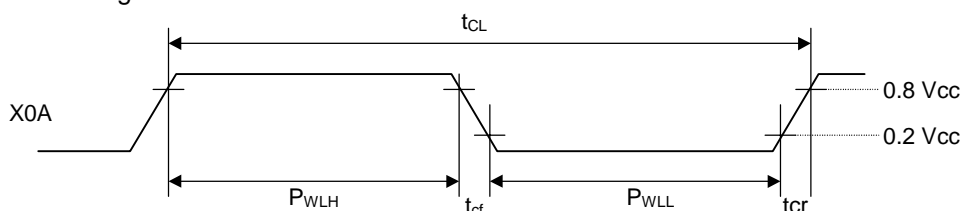
As a guide, set a duty ratio of 30% to 70%.

*3: When using the clock frequency for internal operation at 16 MHz min., use a multiplying circuit. Also, be careful about the operating voltage.

• X0, X1 clock timing

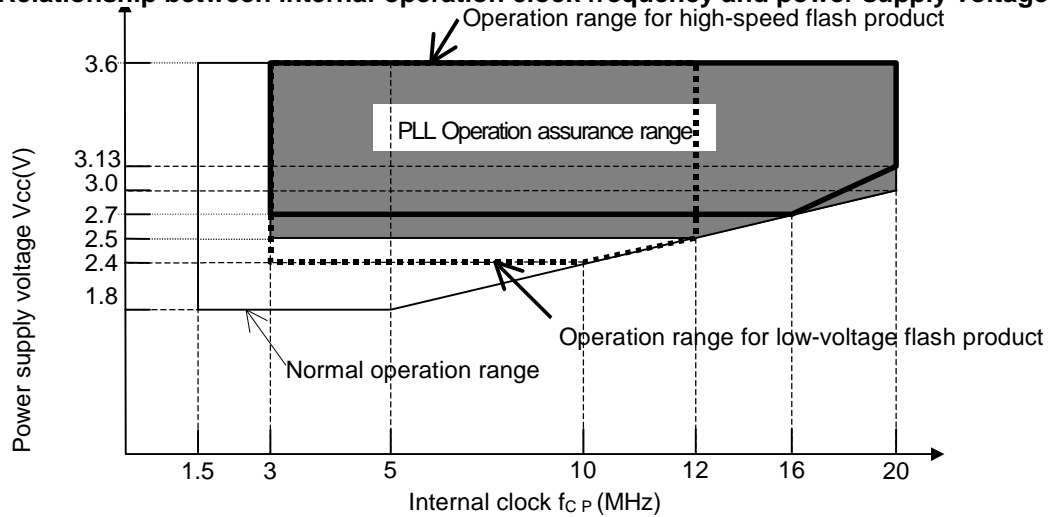


• X0A, X1A clock timing



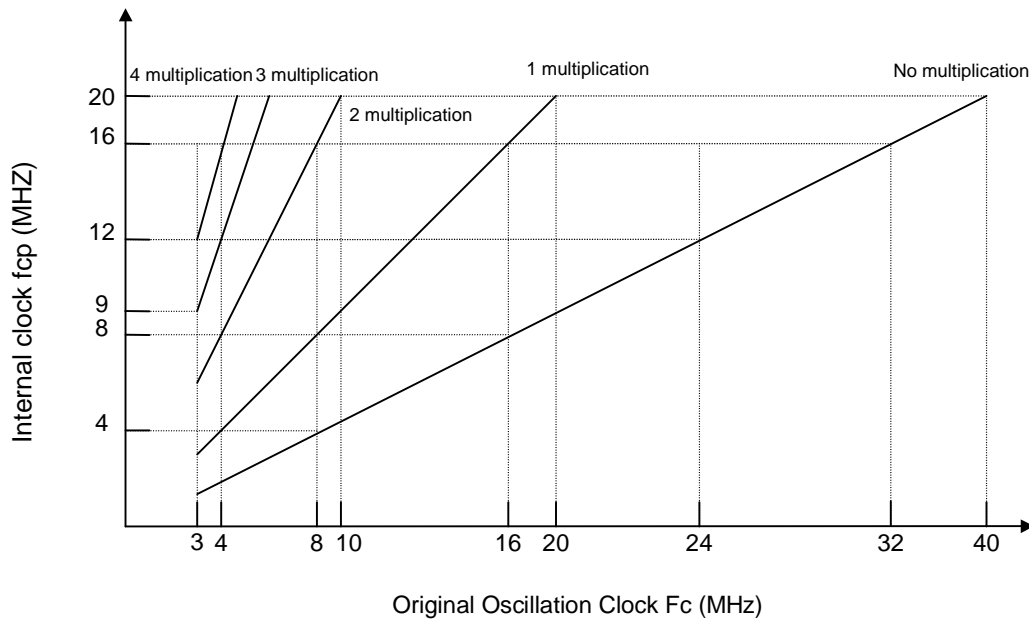
- PLL operating guaranteed range

Relationship between internal-operation clock frequency and power supply voltage



- Notes:**
1. When using a high-speed FLASH product when f is 20 MHz, apply a voltage of 3.13 to 3.6 V.
 2. For the A/D operating frequency, see *the electrical characteristics of the A/D conversion unit*.

Relationship between original oscillation frequency and internal-operation clock frequency

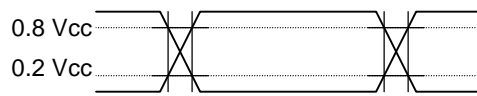


- Note:** When using an internal clock at 16 MHz min., use a frequency multiply circuit (PLL). As a guide, set the upper limit of the original oscillation clock to 20 MHz.

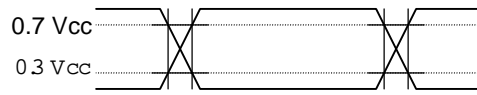
AC specifications are set to the measured reference voltage values below.

- Input signal waveform

Hysterisis input pin

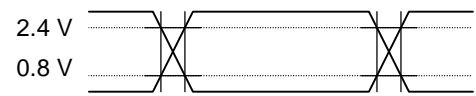


Hysterisis input pin/Pins other than MD



- Output signal waveform

Output pin

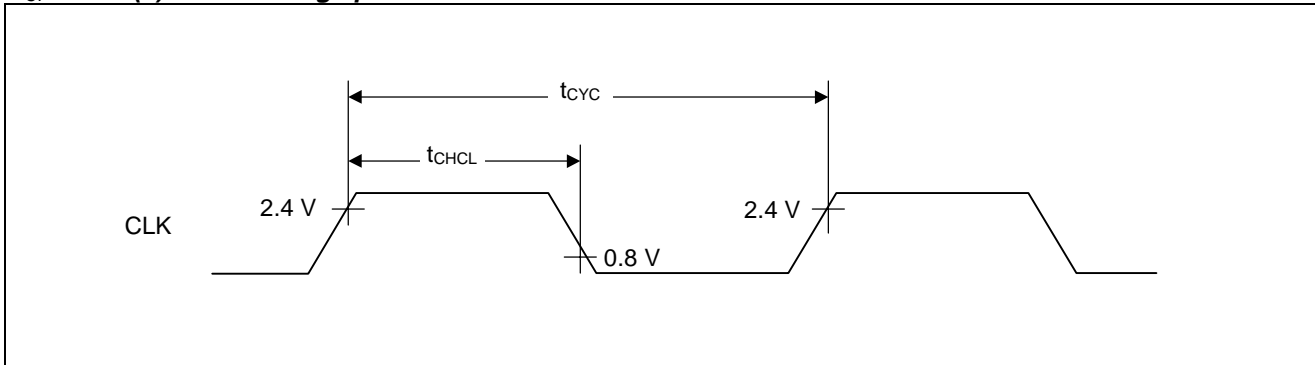


(2) Clock output timing

($V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK		t_{CP}	–	ns	
CLK \uparrow →CLK \downarrow	t_{CHCL}	CLK	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	$t_{CP}/2 - 15$	$T_{CP}/2 + 15$	ns	When $f_{CP} = 20\text{ MHz}$
			$V_{CC} = 2.7\text{ V to }3.3\text{ V}$	$t_{CP}/2 - 20$	$T_{CP}/2 + 20$	ns	When $f_{CP} = 16\text{ MHz}$
			$V_{CC} = 2.7\text{ V to }3.3\text{ V}$	$t_{CP}/2 - 64$	$T_{CP}/2 + 64$	ns	When $f_{CP} = 5\text{ MHz}$

t_{CP} : See (1) Clock timing specifications. *: $V_{CC} = V_{CC3} = V_{CC5}$

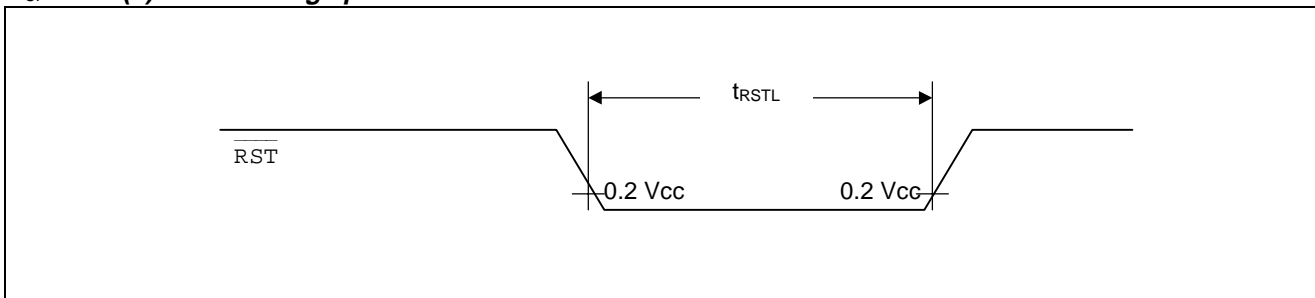


(3) Reset input specifications

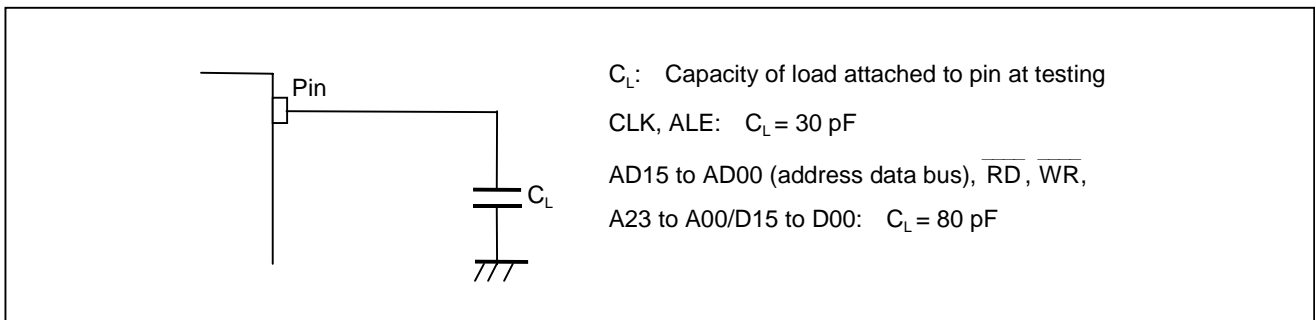
($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	$\overline{\text{RST}}$	–	$16 t_{CP}$	–	ns	

t_{CP} : See (1) Clock timing specifications. *: $V_{CC} = V_{CC3} = V_{CC5}$



Measurement condition for AC specifications



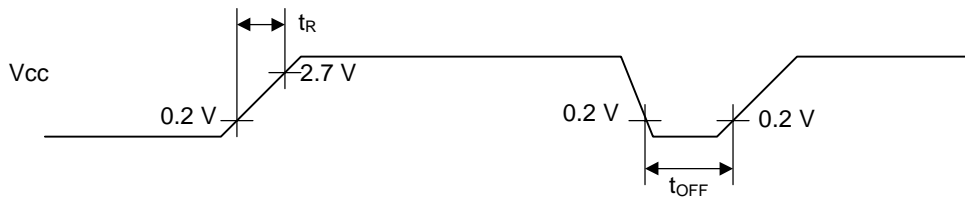
(4) Power-on specifications (power-on reset)

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{ to }+85^\circ\text{C}$)

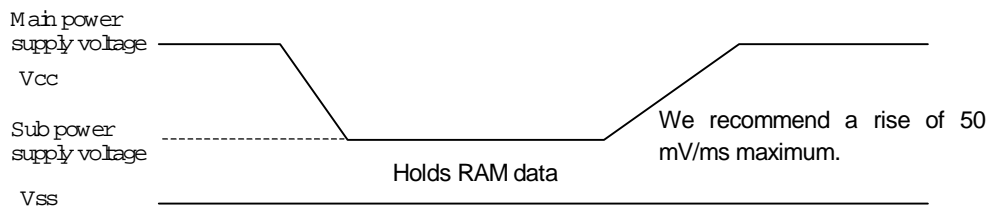
Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
Power supply rise time	t_R	V_{CC}	—	—	30	ms	*
Power supply stop time	t_{OFF}	V_{CC}		1	—	ms	As operation is repeated

*: $V_{CC} < 0.2\text{ V}$ must be given before power-on. *: $V_{CC} = V_{CC3} = V_{CC5}$

- Notes:**
1. The above specifications are numeric values used to trigger a power-on reset.
 2. Perform an internal power-on reset by turning the power on again.



If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

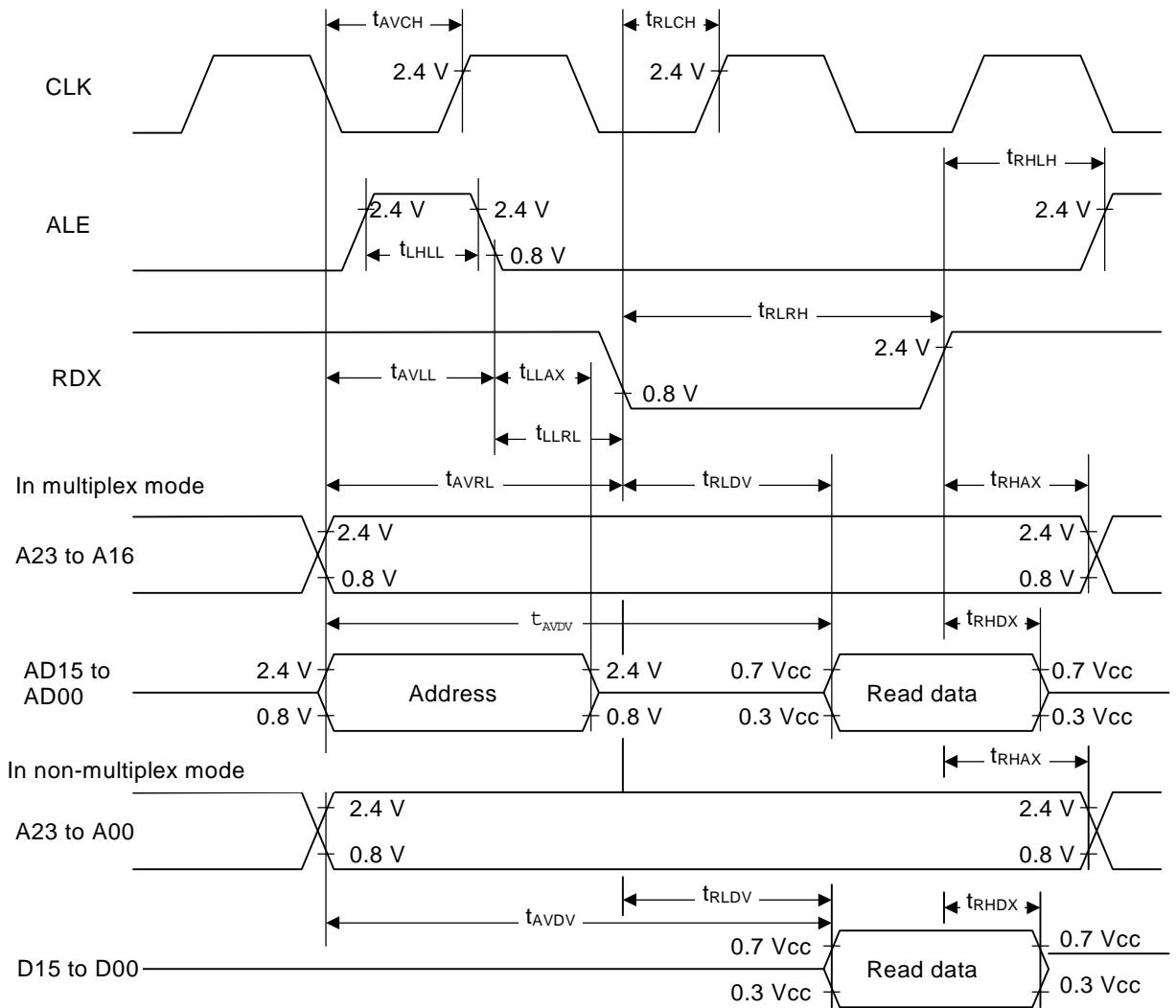


(5) Bus read timing

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = 0^\circ\text{ to }+70^\circ\text{C}$)

Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 15$	—	ns	When $f_{CP} = 20\text{ MHz}$
				$t_{CP}/2 - 20$	—		When $f_{CP} = 16\text{ MHz}$
				$t_{CP}/2 - 35$	—	ns	When $f_{CP} = 8\text{ MHz}$
Valid address \Rightarrow ALE \downarrow time	t_{AVLL}	Address	—	$t_{CP}/2 - 20$	—	ns	
				$t_{CP}/2 - 40$	—		ns
ALE \downarrow \Rightarrow Address valid time	t_{LLAX}	Address	—	$t_{CP}/2 - 15$	—	ns	
Valid address \Rightarrow RDX \downarrow time	t_{AVRL}	RDX, address	—	$t_{CP} - 15$	—	ns	
Valid address \Rightarrow Valid data input	t_{AVDV}	Address/ data	—	—	$5 t_{CP}/2 - 60$	ns	
				—	$5 t_{CP}/2 - 80$		When $f_{CP} = 8\text{ MHz}$
RDXpulse width	t_{RLRH}	RDX	—	$3 t_{CP}/2 - 25$	—	ns	When $f_{CP} = 20\text{ MHz}$
				$3 t_{CP}/2 - 20$	—		ns
RDX \uparrow \Rightarrow Valid data input	t_{RLDV}	Data	—	—	$3 t_{CP}/2 - 60$	ns	
				—	$3 t_{CP}/2 - 80$		When $f_{CP} = 8\text{ MHz}$
RDX \uparrow \Rightarrow data hold time	t_{RHDX}	Data	—	0	—	ns	
RDX \uparrow \Rightarrow ALE \uparrow time	t_{RHLH}	RDX, ALE	—	$t_{CP}/2 - 15$	—	ns	
RDX \uparrow \Rightarrow address valed time	t_{RHAX}	Address, RDX	—	$t_{CP}/2 - 10$	—	ns	
Valid addresss \Rightarrow CLK \uparrow time	t_{AVCH}	Address • CLK	—	$t_{CP}/2 - 20$	—	ns	
RDX \downarrow \Rightarrow CLK \uparrow time	t_{RLCH}	RDX, CLK	—	$t_{CP}/2 - 20$	—	ns	
ALE \downarrow \Rightarrow RDX \downarrow tme	T_{LLRL}	RDX, ALE	—	$t_{CP}/2 - 15$	—	ns	

t_{CP} : See (1) **Clock timing specifications.** *: $V_{CC} = V_{CC3} = V_{CC5}$

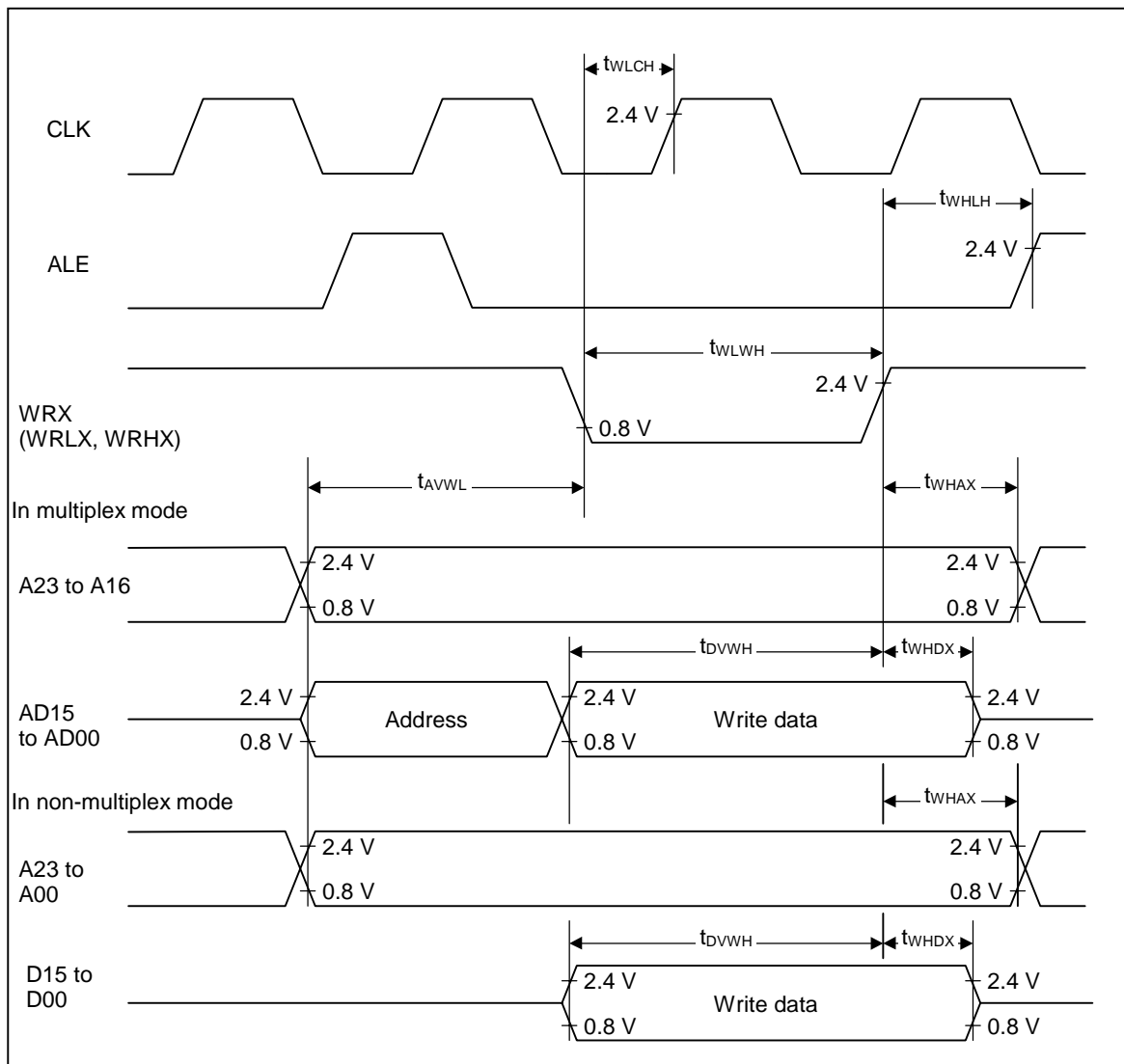


(6) Bus write timing

(• $V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = 0^\circ\text{ to } +70^\circ\text{C}$)

Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
Valid address \Rightarrow WRX \downarrow time	t_{AVWL}	Adress	—	$t_{CP} - 15$	—	ns	
WRX pulse width	t_{WLWH}	WRLX, WRHX	—	$3t_{CP}/2 - 25$	—	ns	When $f_{CP} = 20\text{ MHz}$
			—	$3t_{CP}/2 - 20$	—	ns	When $f_{CP} = 16\text{ MHz}$
Valid data output \Rightarrow WRX \uparrow time	t_{DVWH}	Data	—	$3t_{CP}/2 - 20$	—	ns	
WRX \uparrow • data hold time	t_{WHDX}	Data	—	15	—	ns	When $f_{CP} = 20\text{ MHz}$
			—	20	—	ns	When $f_{CP} = 16\text{ MHz}$
			—	30	—	ns	When $f_{CP} = 8\text{ MHz}$
WRX \uparrow \Rightarrow address valid time	t_{WHAX}	Address	—	$t_{CP}/2 - 10$	—	ns	
WRX \uparrow \Rightarrow ALE \uparrow time	t_{WHLH}	WRX, ALE	—	$t_{CP}/2 - 15$	—	ns	
WRX \downarrow \Rightarrow CLK \uparrow time	t_{WLCH}	WRX, CLK	—	$t_{CP}/2 - 20$	—	ns	

t_{CP} : See (1) Clock timing specifications. *: $V_{CC} = V_{CC3} = V_{CC5}$



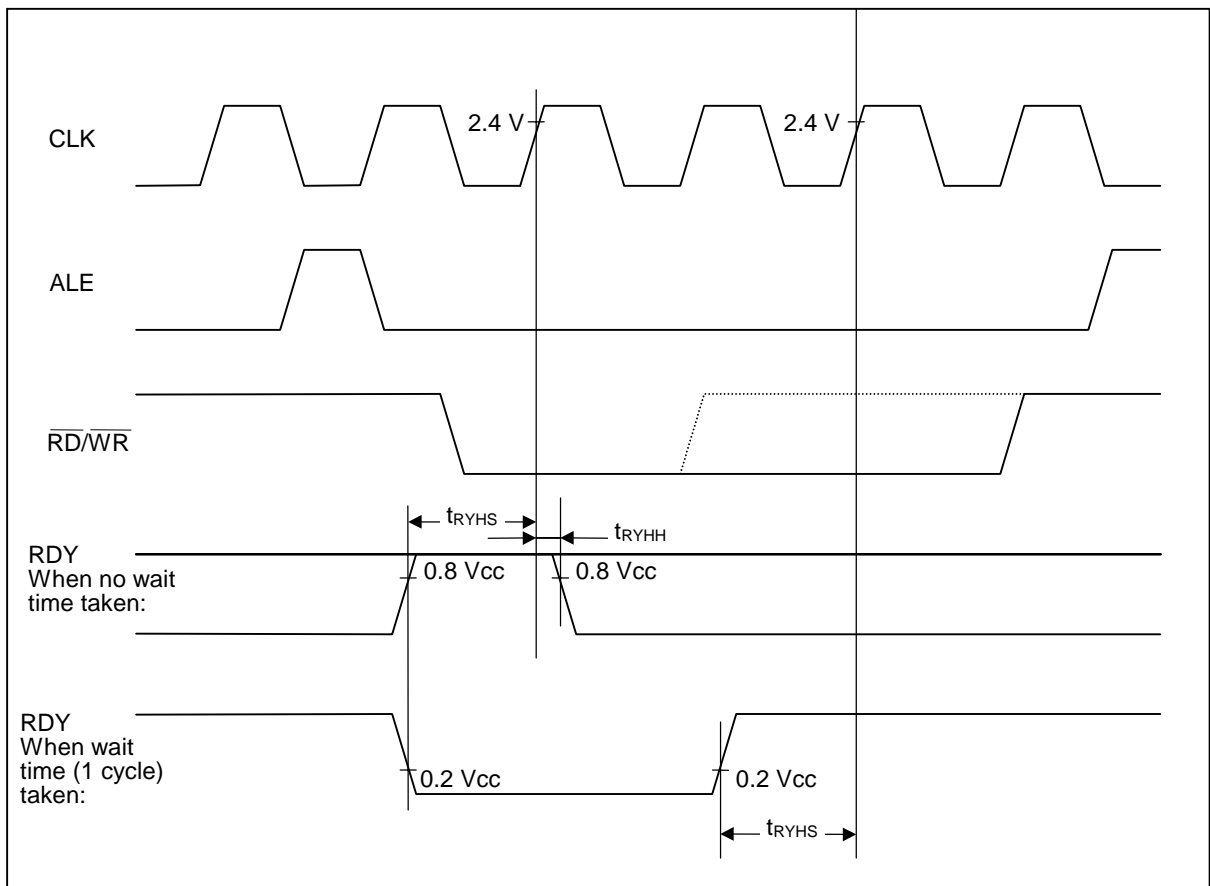
(7) Ready input timing

(V_{CC}= 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A= 0° to +70°C)

Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
RDY Setup time	t _{RYHS}	RDY	—	45	—	ns	f _{CP} = 8 MHz
			—	70	—	ns	
RDY Hold time	t _{RYHH}		—	0	—	ns	

Note: Use auto ready function in case RDY setup time is short.

*:V_{CC} = V_{CC3} = V_{CC5}



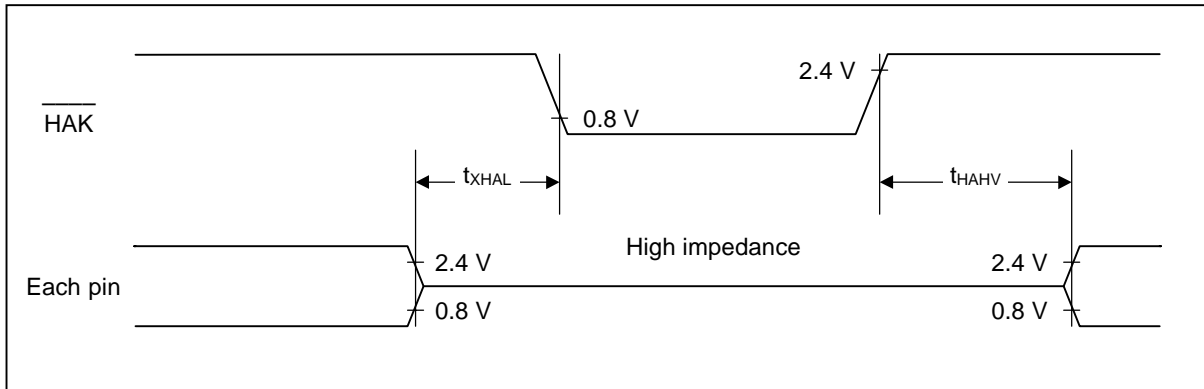
(8) Hold timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = 0° to + 70°C)

Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
Pin floating • $\overline{\text{HAK}}$ • time	t _{XHAL}	$\overline{\text{HAK}}$	—	30	t _{CP}	ns	
$\overline{\text{HAK}} \downarrow \rightarrow$ pin valid time	t _{HAHV}	$\overline{\text{HAK}}$		t _{CP}	2 t _{CP}	ns	

t_{CP}: See (1) **Clock timing specifications.**

Note: The time from the instant the HRQ pin is input to the instant $\overline{\text{HAK}}$ changes is one cycle or more.



(9) UART Timing

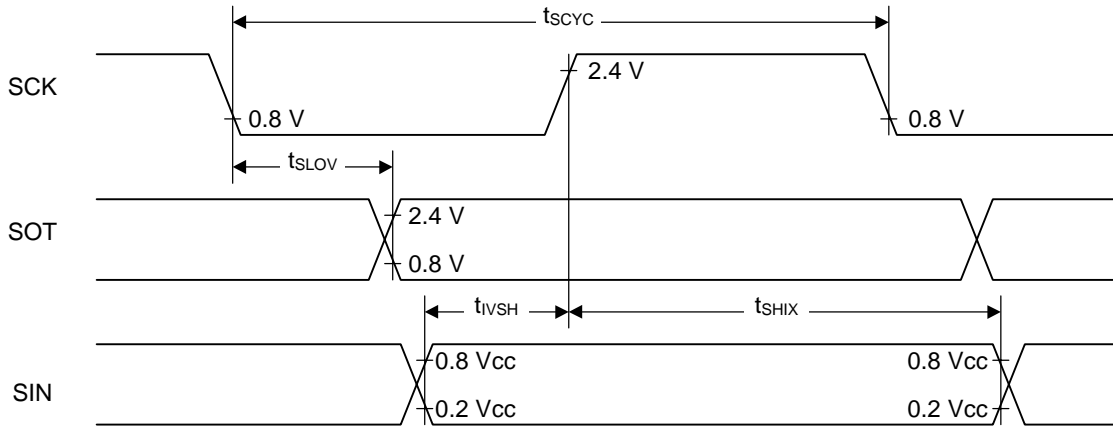
(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = -40° to +85°C)

Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t _{SCYC}	—	For the output pin in the internal shift clock mode, C _L = 80 pF + 1TTL	8t _{CP}	—	ns	
SCK↓→SOT delay time	t _{SLOV}	—		-80	80	ns	
Valid SIN→SCK↑	t _{IVSH}	—		-120	120	ns	f _{CP} = 8 MHz
SCK↑→ Valid SIN hold time	t _{SHIX}	—		100	—	ns	
				200	—	ns	f _{CP} = 8 MHz
Serial clock "H" Pulse width	t _{SHSL}	—	For the output pin in the external shift clock mode, C _L = 80 pF + 1TTL	4 t _{CP}	—	ns	
Serial clock "L" Pulse width	t _{SLSH}	—		4 t _{CP}	—	ns	
SCK↓→SOT delay time	t _{SLOV}	—		—	150	ns	
				—	200	ns	f _{CP} = 8 MHz
Valid SIN→SCK↑	t _{IVSH}	—		60	—	ns	
				120	—	ns	f _{CP} = 8 MHz
SCK↑→ Valid SIN hold time	t _{SHIX}	—		60	—	ns	
				120	—	ns	f _{CP} = 8 MHz

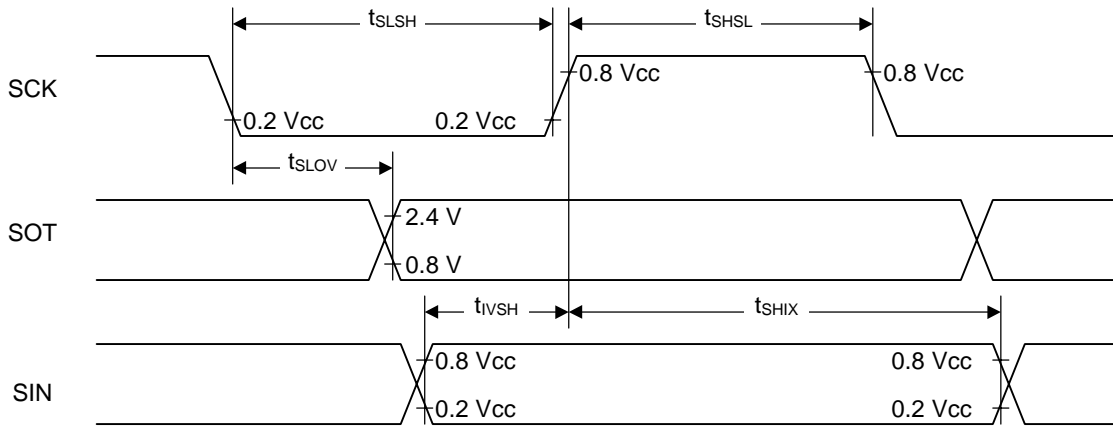
- Notes:**
1. The above values are AC specifications in the CLK synchronous mode.
 2. C_L is the capacity of the load attached to the pin at testing.
 3. t_{CP} is the machine cycle (unit: ns).

*: V_{CC} = V_{CC3} = V_{CC5}

- Internal shift clock mode



- External shift clock mode



(10) I/O extended serial timing

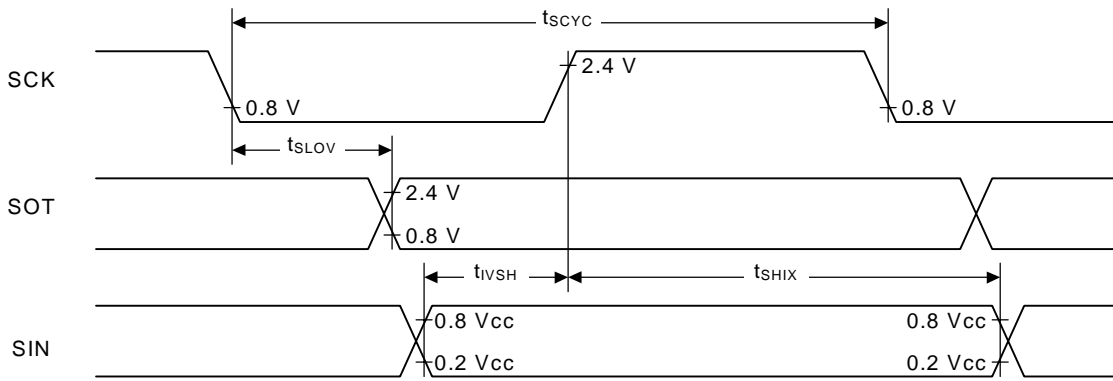
(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = -40° to +85°C)

Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t _{SCYC}	—	For the output pin in the internal shift clock mode, C _L = 80 pF + 1TTL	8t _{CP}	—	ns	
SCK↓→SOT delay time	t _{SLOV}	—		—	80	ns	
Valid SIN→SCK↑	t _{IVSH}	—		—	160	ns	f _{CP} = 8 MHz
SCK↑→ valid SIN hold time	t _{SHIX}	—		t _{CP}	—	ns	
Serial clock "H" Pulse width	t _{SHSL}	—	For the output pin in the external shift clock mode, C _L = 80 pF + 1TTL	230	—	ns	
				460	—	ns	f _{CP} = 8 MHz
Serial clock "L" Pulse width	t _{SLSH}	—		230	—	ns	
				460	—	ns	f _{CP} = 8 MHz
SCK↓→SOT delay time	t _{SLOV}	—		—	2 t _{CP}	ns	
Valid SIN→SCK↑	t _{IVSH}	—		t _{CP}	—	ns	
SCK↑→ Valid SIN hold time	t _{SHIX}	—		2t _{CP}	—	ns	

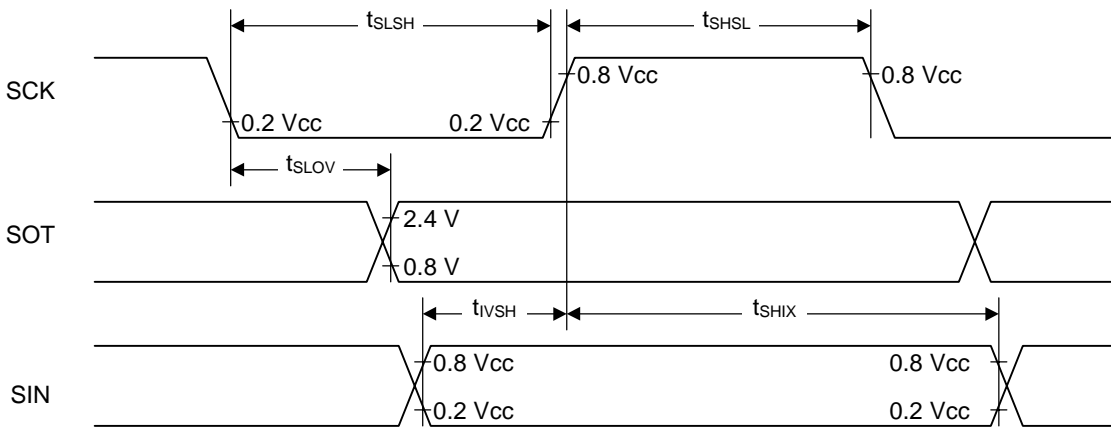
- Notes:**
1. The above values are AC specifications in the CLK synchronous mode.
 2. C_L is the capacity of the load attached to the pin at testing.
 3. t_{CP} is the machine cycle (unit: ns).
 4. Values in the table are target value.

*: V_{CC} = V_{CC3} = V_{CC5}

- Internal sift clock mode



- External sift clock mode

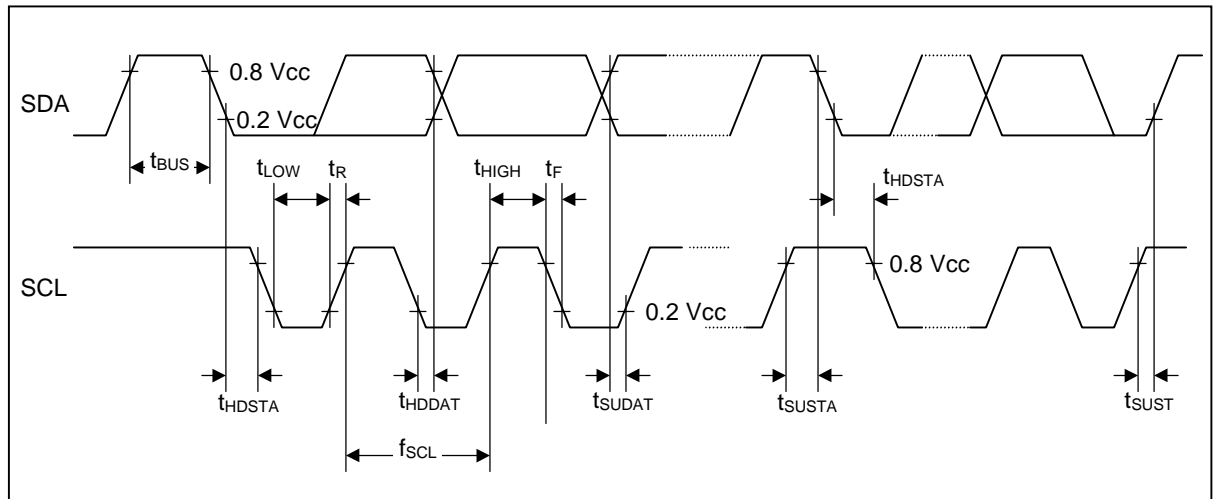


(11) I²C timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = -40° to + 85°C)

Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
SCL Clock frequency	f _{SCL}	—	—	0	100	kHz	
Bus-free time between stop and start conditions	t _{BUS}	—		4.7	—	μs	
Start of hold time (start of retransmission)	t _{HDSTA}	—		4.0	—	μs	The first clock pulse is generated after this period has elapsed.
SCL Clock LOW state hold time	t _{LOW}	—		4.7	—	μs	
SCL Clock HIGH state hold time	t _{HIGH}	—		4.0	—	μs	
Setup time for retransmission start condition	t _{SUSTA}	—		4.7	—	μs	
Data hold time	t _{HDDAT}	—		0	—	μs	
Data setup time	t _{SUDAT}	—		40	—	ns	
SDA/SCL Signal rise time	t _R	—		—	1000	ns	
SDA/SCL Signal fall time	t _F	—		—	300	ns	
Stop condition setup time	t _{SUSTO}	—		4.0	—	μs	

*: V_{CC} = V_{CC3} = V_{CC5}

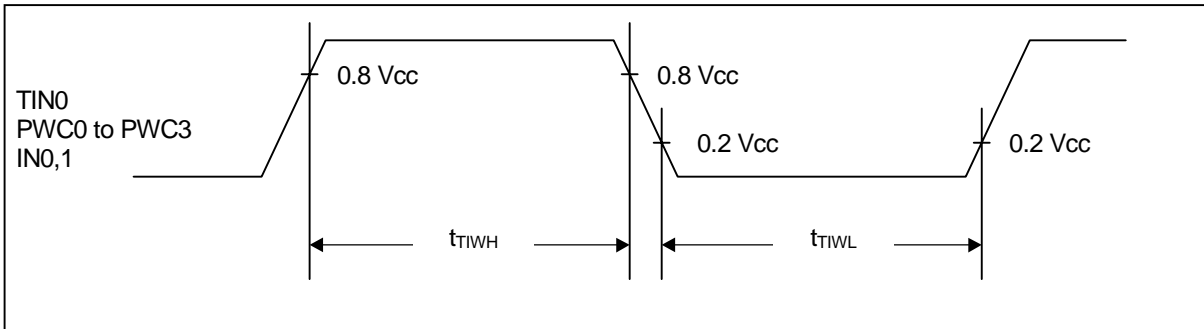


(12) Timer input timing

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{ to }+85^\circ\text{C}$)

Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 IN0, 1 PWC0 to PWC3	—	$4 t_{CP}$	—	ns	

*: $V_{CC} = V_{CC3} = V_{CC5}$

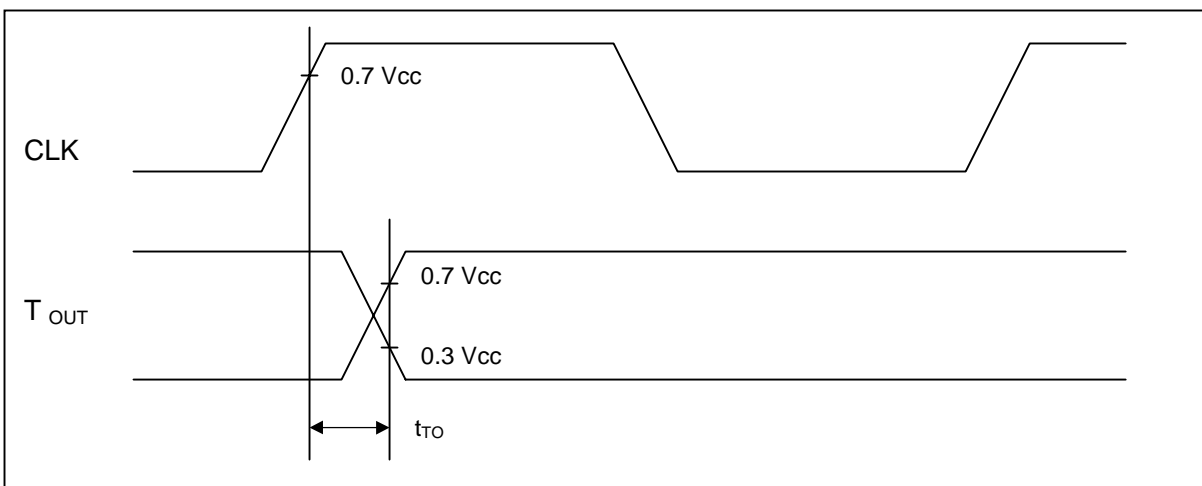


(13) Timer output timing

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{ to }+85^\circ\text{C}$)

Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
$CLK \uparrow \rightarrow T_{OUT}$ change time	t_{TO}	TOT0 PPG0 to PPG5 OUT0 to 5	Load: 80 pF	30	—	ns	

*: $V_{CC} = V_{CC3} = V_{CC5}$

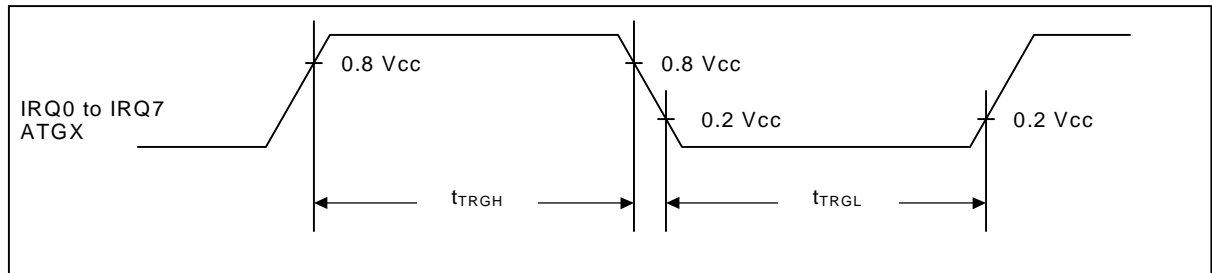


(14) Trigger input timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = -40° to +85°C)

Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
Input pulse width	t _{TRGH} t _{TRGL}	ATGX IRQ0 to IRQ7	—	5 t _{CP}	—	ns	

*: V_{CC} = V_{CC3} = V_{CC5}

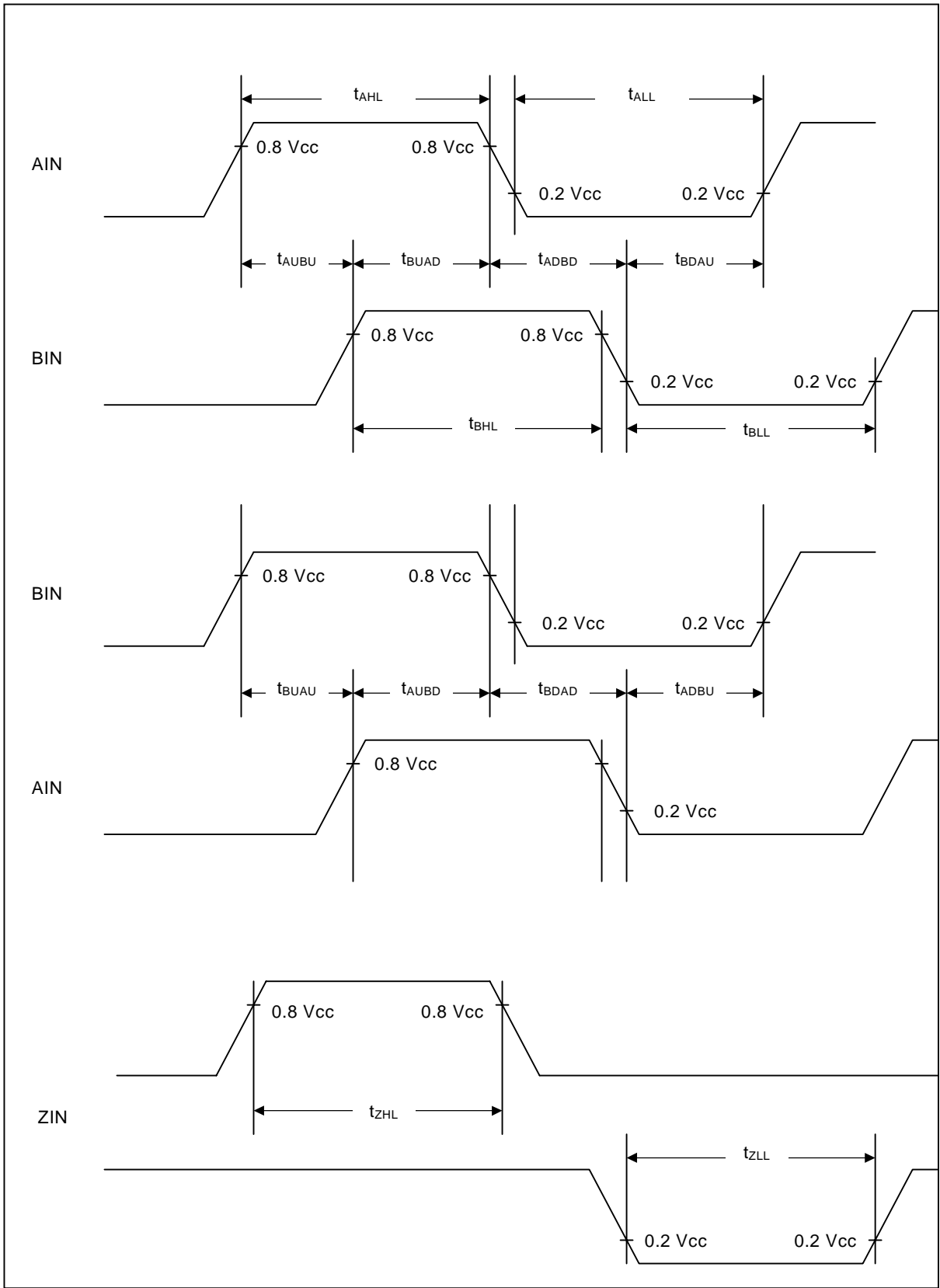


(15) Updown counter timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = -40° to +85°C)

Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
AIN Input "H" pulse width	t _{AHL}	AIN0, AIN1 BIN0, BIN1	Lord: 80 pF	8 t _{CP}	—	ns	
AIN Input "L" pulse width	t _{ALL}			8 t _{CP}	—	ns	
BIN Input "H" pulse width	t _{BHL}			8 t _{CP}	—	ns	
BIN Input "L" pulse width	t _{BLL}			8 t _{CP}	—	ns	
AIN↑→BIN↑time	t _{AUBU}			4 t _{CP}	—	ns	
BIN↑→AIN↓time	t _{BUAD}			4 t _{CP}	—	ns	
AIN↓→BIN↑ time	t _{ADBD}			4 t _{CP}	—	ns	
BIN↓→AIN↑ time	t _{BDAU}			4 t _{CP}	—	ns	
BIN↑→AIN↑ time	t _{BUAU}			4 t _{CP}	—	ns	
AIN↑→BIN↓ time	t _{AUBD}			4 t _{CP}	—	ns	
BIN↓→AIN↑ time	t _{BDAD}			4 t _{CP}	—	ns	
AIN↓→BIN↑ time	t _{ADBU}			4 t _{CP}	—	ns	
ZIN Input "H" pulse width	t _{ZHL}	ZIN0, ZIN1		4 t _{CP}	—	ns	
ZIN Input "L" pulse width	t _{ZLL}			4 t _{CP}	—	ns	

*: V_{CC} = V_{CC3} = V_{CC5}

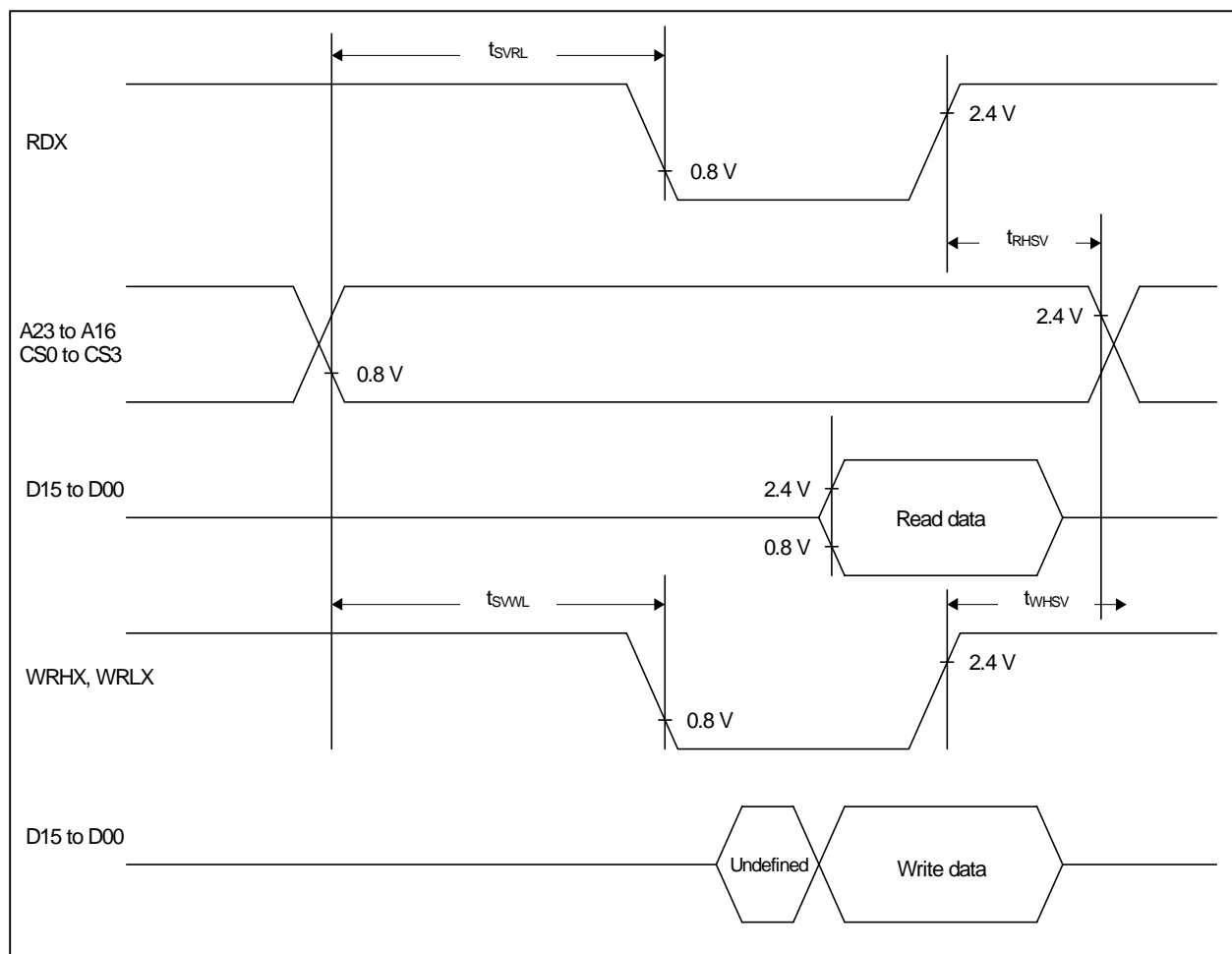


(16) Chip select output timing

(Vcc = 2.7 V to 3.6 V, Vss = 0.0 V, TA = -40° to +85°C)

Parameter	Symbol	Pin	Test condition	Rated value		Unit	Remarks
				Min.	Max.		
Chip select output valid time→ RDX ↓	t _{SVRL}	CS0 to CS3 RDX	—	t _{CP/2-10}		ns	
Chip select output valid time→ WRX ↓	t _{SVWL}	CS0 to CS3 WRHX, WRLX		t _{CP/2-10}		ns	
RDX ↑→ Chip select output valid time	t _{RHSV}	RDX CS0 to CS3	—	t _{CP/2-20}		ns	
WRX ↑→ Chip select output valid time	t _{WHSV}	WRHX, WRLX CS0 to CS3	—	t _{CP/2-20}	—	ns	

*: Vcc = Vcc3 = Vcc5



Note: There is a possibility of a bus conflict because Chip Select output signals change concurrently due to the configuration of the internal bus.

AC cannot be ensured between the ALE output signal and the Chip Select output signal.

5. A/D Conversion Unit Electrical Characteristics

($V_{CC} = AV_{CC} = 2.2$ to 3.6 V, $V_{SS} = AV_{SS} = 0.0$ V, 2.2 V \leq AVRH, $T_A = -40^\circ$ to $+85^\circ$ C)

Parameter	Symbol	Pin	Rated value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	10	10	bit	
Overall error	—	—	—	—	± 3.0	LSB	
Linearity error	—	—	—	—	± 2.5	LSB	
Differential linearity error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	$AV_{SS} - 1.5$ LSB	$AV_{SS} + 0.5$ LSB	$AV_{SS} + 2.5$ LSB	mV	
Full scale transition voltage	V_{FST}	AN0 to AN7	$AVRH - 3.5$ LSB	$AVRH - 1.5$ LSB	$AVRH + 0.5$ LSB	mV	
Conversion time	—	—	5.8125^{*1}	—	—	μ s	When AVRH \geq 2.7 V
Analog port input current	I_{AIN}	AN0 to AN7	—	0.1	10	μ A	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	—	AVRH	V	
Reference voltage	—	AVRH	$AV_{SS} + 2.2$	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	1.2	4.4	mA	
	I_{AH}	AV_{CC}	—	—	5^{*3}	μ A	
Reference voltage supply current	I_R	AVRH	—	95	170	μ A	
	I_{RH}	AVRH	—	—	5^{*2}	μ A	
Channel differences	—	AN0 to AN7	—	—	4	LSB	

*1: At 16-MHz machine clock

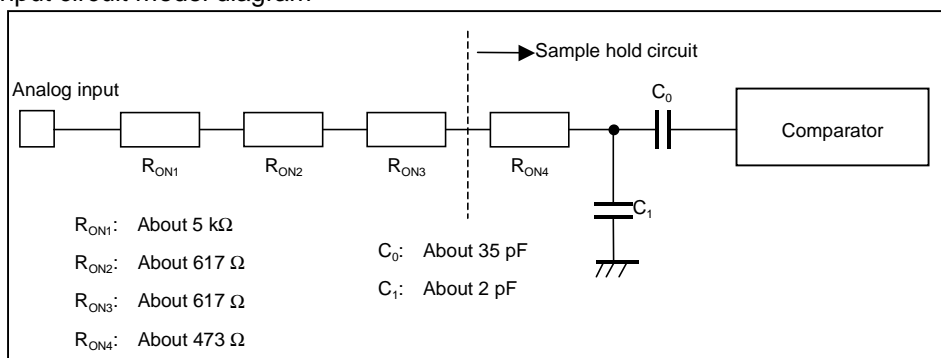
*2: When not operating A/D converter, this is the current ($V_{CC} = AV_{CC} = AVRH = 3.0$ V) when the CPU is stopped.

*3: $V_{CC} = V_{CC3} = V_{CC5}$

Notes:

- The error is relatively large as the $|AVRH - AV_{SS}|$ becomes smaller.
- Analog input external circuit output impedance should use the following conditions.
External Circuit Output Impedance ≤ 6 k Ω
When using an external capacitor, it's capacity should be a few thousand times the capacity of the internal capacitor, considering the effect of the external capacitor and the effect of the divided voltage of the capacity of the internal capacitor.
- If the external circuit output impedance is too high, there maybe insufficient time for sampling of the analog voltage (sampling time = 3.75 μ s at machine clock of 16 MHz).

• Analog input circuit model diagram



Note: The above values are a guide.

($V_{CC} = 1.8\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $1.8\text{ V} \leq AV_{RH}$, $T_A = -40^\circ\text{ to }+85^\circ\text{C}$)

Parameter	Symbol	Pin	Rated value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	10	10	bit	
Overall error	—	—	—	—	± 4.0	LSB	
Linearity error	—	—	—	—	± 3.5	LSB	
Differential linearity error	—	—	—	—	± 2.4	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	$AV_{SS} - 2.0\text{ LSB}$	$AV_{SS} + 0.5\text{ LSB}$	$AV_{SS} + 3.0\text{ LSB}$	mV	
Full scale transition voltage	V_{FST}	AN0 to AN7	$AV_{RH} - 4.0\text{ LSB}$	$AV_{RH} - 1.5\text{ LSB}$	$AV_{RH} + 1.0\text{ LSB}$	mV	
Conversion time	—	—	5.8125^{*1}	—	—	μs	When $AV_{RH} \geq 2.7\text{ V}$
Analog port input current	I_{AIN}	AN0 to AN7	—	0.1	10	μA	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	—	AV_{RH}	V	
Reference voltage	—	AV_{RH}	$AV_{SS} + 1.8$	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	1.2	4.4	mA	
	I_{AH}	AV_{CC}	—	—	5^{*3}	μA	
Reference voltage supply current	I_R	AV_{RH}	—	95	170	μA	
	I_{RH}	AV_{RH}	—	—	5^{*2}	μA	
Channel differences	—	AN0 to AN7	—	—	4	LSB	

*1: At 16-MHz machine clock

*2: When not operating A/D converter, this is the current ($V_{CC} = AV_{CC} = AV_{RH} = 3.0\text{ V}$) when the CPU is stopped.

*3: $V_{CC} = V_{CC3} = V_{CC5}$

Restrictions on A/D operation frequency (for information)

Power supply voltage	A/D Conversion time [μs]	Machine clock
$3.6\text{ V} \geq AV_{CC} \geq 3.0\text{ V}$	4.650	20 MHz
$3.6\text{ V} \geq AV_{CC} \geq 2.7\text{ V}$	5.813	16 MHz
$2.7\text{ V} > AV_{CC} \geq 2.6\text{ V}$	6.643	14 MHz
$2.6\text{ V} > AV_{CC} \geq 2.5\text{ V}$	7.750	12 MHz
$2.5\text{ V} > AV_{CC} \geq 2.4\text{ V}$	8.445	11 MHz
$2.4\text{ V} > AV_{CC} \geq 2.3\text{ V}$	9.300	10 MHz
$2.3\text{ V} > AV_{CC} \geq 2.2\text{ V}$	11.63	8 MHz
$2.2\text{ V} > AV_{CC} \geq 2.1\text{ V}$	15.50	6 MHz
$2.1\text{ V} > AV_{CC} \geq 2.0\text{ V}$	23.25	4 MHz
$2.0\text{ V} > AV_{CC} \geq 1.9\text{ V}$	46.50	2 MHz
$1.9\text{ V} > AV_{CC} \geq 1.8\text{ V}$	93.00	1 MHz

6. Handling Device

- **Preventing latch-up**

Latch-up may occur in CMOSIC when a voltage higher than V_{cc} or lower than V_{ss} is applied to other than the middle/high withstandable voltage input or output pins, or a voltage exceeding the rated value is applied between V_{cc} and V_{ss} . Latch-up may cause a rapid increase in the supply current, sometimes resulting in thermal damage to the device. Therefore, keep the used voltage within the maximum ratings.

When turning the power on and off the analog supply voltage (AV_{cc} , $AVRH$) analog input should not exceed the digital supply voltage (V_{cc}).

- **Voltage supplies should be stabilized.**

A sudden change of the power supply voltage may cause a malfunction even within the guaranteed range of operation of the power supply voltage. For reference of stabilization, voltage variations are recommended to be restrained so that V_{cc} ripple variations (P-P values) are below 10% of the standard V_{cc} value in commercial frequencies (50 to 60 Hz), and so that transient variation is below 0.1 V/ms in sudden changes during power switchovers.

- **Precautions when turning on the power supply**

Ensure a minimum of 50 ms (between 0.2 to 2.7 V) for voltage rise times when turning on the power supply to prevent malfunction of the built-in power reduction circuit.

- **Handling of N.C. pins**

Always leave N.C. pins (internal connections) open.

- **Handling of power supply pins for product with A/D converters**

Connect power supply pins with $AV_{cc} = AVRH = V_{cc}$, $AV_{ss} = V_{ss}$ even when not using the A/D converters.

- **Precautions when using the external clock**

Oscillating stability waiting time is required when resetting from the Power On Reset, Sub-clock Mode and Stop Mode when using the external clock. As a guide, when using an external clock, set its upper limit to 20 MHz.

- **Order of turning on the power**

Turn off the digital power supply (V_{cc}) after turning off the A/D converter power supplies (AV_{cc} , $AVRH$) and analog input ($AN0$ to $AN7$).

Do not allow the $AVRH$ to exceed AV_{cc} when turning the power on and off.

Do not allow the input voltage to exceed AV_{cc} when using the analog input pins as an input port.

Note: $V_{cc} = V_{cc3} = V_{cc5}$

- **Note that low-voltage FLASH products (2.4 V to 3.6 V/10 MHz) do not have the security function.**

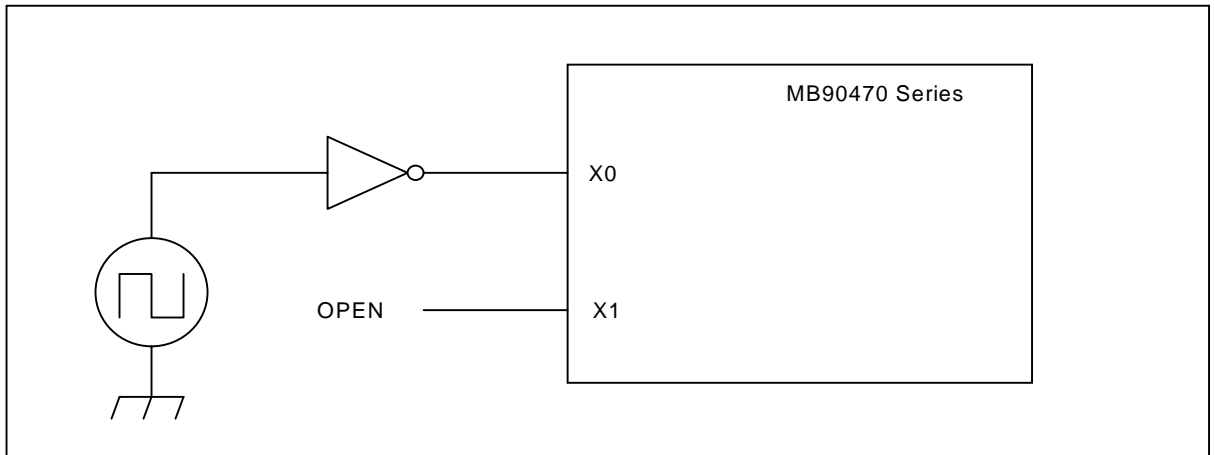
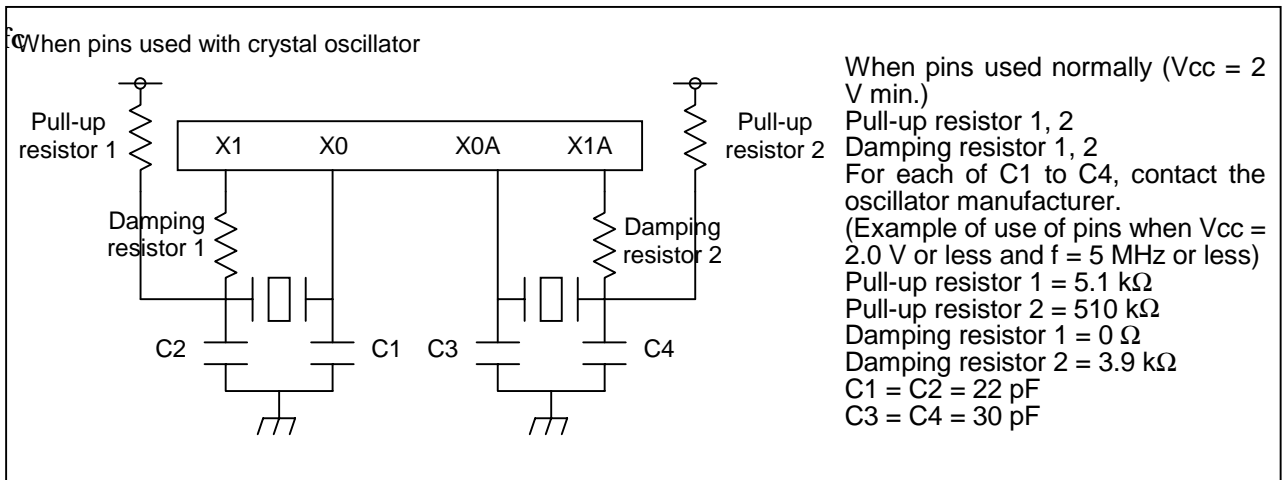
- **Handling unused pins**

If unused input pins are left open, this may cause a malfunction or latch-up, resulting in permanent damage. Use a pull-up or pull-down resistor of 2 k Ω min. Also, when there are unused I/O pins, set them to the output state and free them, or set them to the input state and handle them in the same way as input pins.

- **Caution when using external crystal oscillator**

As a guide, set the upper limit to 20 MHz. To use the 16-MHz internal clock, use the PLL multiply.

- Usage of X0/X1 and X0A/X1A



Example of use of pins as external clock input pins