

# 16-bit Proprietary Microcontroller

CMOS

## F<sup>2</sup>MC-16LX MB90340 Series

**MB90F342/C(S), MB90F344/C(S), MB90F347/C(S),  
MB90341/C(S), MB90342/C(S), MB90343/C(S),  
MB90344/C(S), MB90346/C(S), MB90347/C(S),  
MB90348/C(S), MB90349/C(S), MB90V340(S)**

### ■ DESCRIPTION

The MB90340-series with up to two FULL-CAN interfaces (MB90V340: 3ch) and FLASH ROM is especially designed for automotive and industrial applications. Its main features are the on board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach. With the new 0.35  $\mu\text{m}$  CMOS technology, Fujitsu now offers on-chip FLASH-ROM program memory up to 384 Kbytes. An internal voltage booster removes the necessity for a second programming voltage.

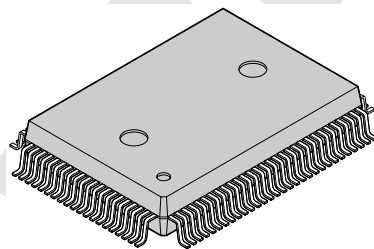
An on board voltage regulator provides 3 V to the internal MCU core. This creates a major advantage in terms of EMI and power consumption.

The internal PLL clock frequency multiplier provides an internal 42 ns instruction cycle time from an external 4 MHz clock.

The unit features an 8 channel Output Compare Unit and 8channel Input Capture Unit with two separate 16-bit free running timers. 4 UARTs (MB90V340: 5 UARTs) constitute additional functionality for communication purposes.

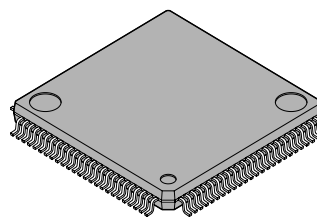
### ■ PACKAGE

100-pin Plastic QFP



(FPT-100P-M06)

100-pin Plastic LQFP



(FPT-100P-M05)

## ■ FEATURES

- 16-bit core CPU; 4 MHz external clock (24 MHz internal, 42 ns instr. cycle time)
- New 0.35  $\mu\text{m}$  CMOS Process Technology
- Internal voltage regulator supports 3 V MCU core, offering low EMI and low power consumption figures
- Up to two FULL-CAN\*<sup>1</sup> interfaces (MB90V340: 3ch); conforming to Version 2.0 Part A and Part B, flexible message buffering (mailbox and FIFO buffering can be mixed)
- Powerful interrupt functions (8 progr. priority levels; 16 external interrupts)
- EI2OS - Automatic transfer function indep.of CPU; 16 ch. of intelligent I/O Services
- DMA
- 18-bit Time-base counter
- Watchdog Timer
- 4 full duplex UARTs (SCI/LIN) (MB90V340: 5 UARTs)
- Up to 2 ch I<sup>2</sup>C with 400 kbit/s
- A/D Converter : 16 ch to 24 ch. analog inputs (Resolution 10 bits or 8 bit, conversion time 3 $\mu\text{s}$ )
- 16-bit reload timer  $\times 4$  ch
- ICU (Input capture) 16 bit $\times 8$  ch
- OCU (Output capture) 16 bit $\times 8$  ch
- 16-bit free running timer $\times 2$  ch (FRT0 : ICU 0/1/2/3, OCU 0/1/2/3, FRT1 : ICU 4/5/6/7, OCU 4/5/6/7)
- 8/16-bit Programmable Pulse Generator 8ch $\times 16$ -bit / 16ch $\times 8$ -bit
- Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)
- 4-byte instruction execution queue
- signed multiply (16 bit $\times 16$  bit) and divide (32 bit/16 bit) instructions available
- Program Patch Function
- Fast Interrupt processing
- Low Power Consumption - 10 different power saving modes : (Sleep, Stop, CPU intermittent mode, ...)
- Up to 100kHz\*<sup>2</sup> Subsystem Clock (devices without S-suffix)
- External bus interface
- Programmable input levels (Automotive / CMOS-Schmitt (initial level is Automotive), for external bus also TTL level)
- Package : 100-pin plastic QFP and LQFP

(\*1) Controller Area Network (CAN) - License of Robert Bosch GmbH

(\*2) When use watch timer function, input 32.768kHz clock to XA0(/XA1) pin.

## ■ PRODUCT LINEUP

Part Number	MB90F342/C(S) <sup>*1</sup> , MB90F344/C(S) <sup>*1</sup> , MB90F347/C(S), MB90341/C(S) <sup>*1</sup> , MB90342/C(S) <sup>*1</sup> , MB90343/C(S) <sup>*1</sup> , MB90344/C(S) <sup>*1</sup> , MB90346/C(S) <sup>*1</sup> , MB90347/C(S), MB90348/C(S) <sup>*1</sup> , MB90349/C(S) <sup>*1</sup>	MB90V340(S)
CPU	F <sup>2</sup> MC-16LX CPU	
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, ×8, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz osc. PLL ×6)	
ROM	Boot-block, Flash memory 384Kbytes : MB90F344/C(S), MB90344/C(S), MB90343/C(S) 256Kbytes : MB90349/C(S), MB90F342/C(S), MB90342/C(S) 128Kbytes : MB90F347/C(S), MB90347/C(S), MB90348/C(S), MB90341/C(S) 64Kbytes : MB90346/C(S)	External
RAM	30Kbytes : MB90F344/C(S), MB90344/C(S) 20Kbytes : MB90343/C(S) 16Kbytes : MB90349/C(S), MB90348/C(S), MB90F342/C(S), MB90342/C(S), MB90341/C(S) 6Kbytes : MB90F347/C(S), MB90347/C(S) 2Kbytes : MB90346/C(S)	30 Kbytes
Emulator-specific power supply <sup>*2</sup>	—	None
Technology	0.35 μm CMOS with on-chip voltage regulator for internal power supply + Flash memory with On-chip charge pump for programming voltage	0.35 μm CMOS with on-chip voltage regulator for internal power supply
Operating voltage range	3.5 - 5.5 V (4.0 - 5.5 V if A/D Converter is used)	5 V ± 10%
Temperature range	−40 °C to 105	—
Package	QFP-100, LQFP-100	PGA-299
UART	4 channels	5channels
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device	
I <sup>2</sup> C (400 kbit/s)	devices with 'C'-suffix: 2ch devices without 'C'-suffix: —	2 channel
A/D Converter	devices with 'C'-suffix: 24ch devices without 'C'-suffix: 16ch	24 input channels
	10-bit or 8-bit resolution Conversion time : Min 3 μs include sample time (per one channel)	
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2 <sup>1</sup> , fsys/2 <sup>3</sup> , fsys/2 <sup>5</sup> (fsys = System clock frequency) Supports External Event Count function	
16-bit I/O Timer (2 channels)	Signals an interrupt when overflowing Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : fsys, fsys/2 <sup>1</sup> , fsys/2 <sup>2</sup> , fsys/2 <sup>3</sup> , fsys/2 <sup>4</sup> , fsys/2 <sup>5</sup> , fsys/2 <sup>6</sup> , fsys/2 <sup>7</sup> (fsys = System clock freq.) I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1/2/3, OCU 0/1/2/3 I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7	

# MB90340 Series

(continued)

Part Number	MB90F342/C(S) <sup>*1</sup> , MB90F344/C(S) <sup>*1</sup> , MB90F347/C(S), MB90341/C(S) <sup>*1</sup> , MB90342/C(S) <sup>*1</sup> , MB90343/C(S) <sup>*1</sup> , MB90344/C(S) <sup>*1</sup> , MB90346/C(S) <sup>*1</sup> , MB90347/C(S), MB90348/C(S) <sup>*1</sup> , MB90349/C(S) <sup>*1</sup>	MB90V340(S)
Parameter		
16-bit Output Compare (8 channels)	Signals an interrupt when a match with 16-bit I/O Timer 16-bit compare registers. A pair of compare registers can be used to generate an output signal.	
16-bit Input Capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Signals an interrupt upon external event	
8/16-bit Programmable Pulse Generator (8 channels)	Supports 8-bit and 16-bit operation modes Sixteen 8-bit reload counters Sixteen 8-bit reload registers for L pulse width Sixteen 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operation clock freq. : fsys, fsys/2 <sup>1</sup> , fsys/2 <sup>2</sup> , fsys/2 <sup>3</sup> , fsys/2 <sup>4</sup> or 102.4 μs@fosc = 5 MHz (fsys = System clock frequency, fosc = Oscillation clock frequency)	
CAN Interface	2 ch : MB90F344/C(S), MB90344/C(S), MB90343/C(S), MB90F342/C(S), MB90342/C(S), MB90341/C(S) 1 ch : MB90349/C(S), MB90348/C(S), MB90F347/C(S), MB90347/C(S), MB90346/C(S)	3 channels
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps	
External Interrupt (16 channels)	Can be programmed edge sensitive or level sensitive	
D/A converter	—	2 channels
Up to 100kHz Sub-clock for low power operation	devices without 'S'-suffix: yes devices with 'S'-suffix: —	
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs Bit-wise programmable as input/output or peripheral signal Programmable in groups of 8 as CMOS schmitt trigger/ automotive inputs (default) TTL input level programmable for external bus (default for external reset vector fetch)	

Part Number Parameter	MB90F342/C(S) <sup>*1</sup> , MB90F344/C(S) <sup>*1</sup> , MB90F347/C(S), MB90341/C(S) <sup>*1</sup> , MB90342/C(S) <sup>*1</sup> , MB90343/C(S) <sup>*1</sup> , MB90344/C(S) <sup>*1</sup> , MB90346/C(S) <sup>*1</sup> , MB90347/C(S), MB90348/C(S) <sup>*1</sup> , MB90349/C(S) <sup>*1</sup>	MB90V340(S)
Flash Memory	Supports automatic programming, Embedded Algorithm™ <sup>*3</sup> Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash	—

\*1 : The devices other than MB90F347/C(S) and MB90347/C(S) are under development.

\*2 : It is setting of Jumper switch SI when Emulation Pod (MB2147) is used.  
Please refer to the Emulator hardware manual about details.

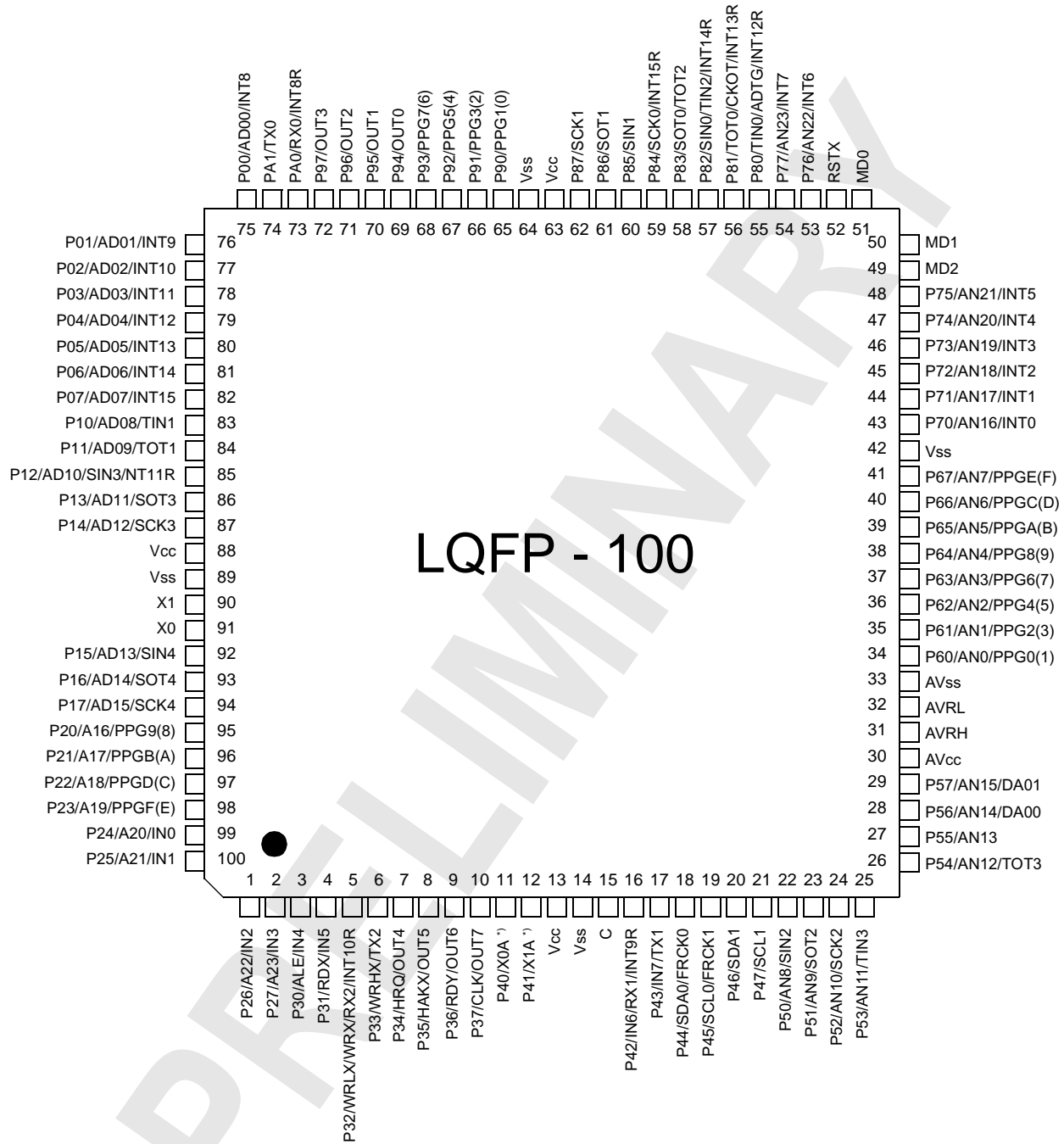
\*3 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

PRELIMINARY



- MB90V340(S) as seen with probe cable for LQFP100

(TOP VIEW)



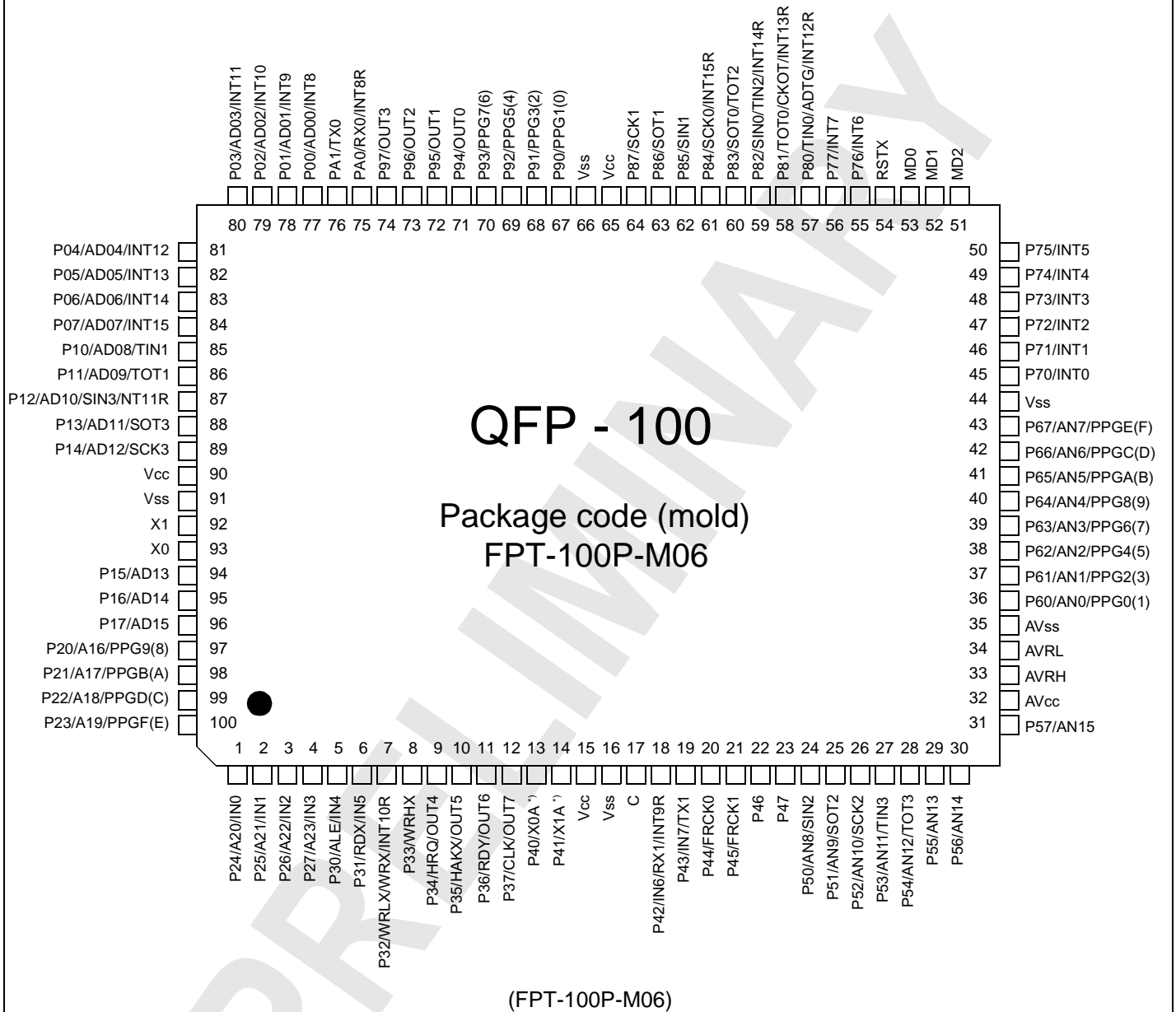
(FPT-100P-M05)

\*) MB90V340: X0A, X1A  
 MB90V340S: P40, P41

# MB90340 Series

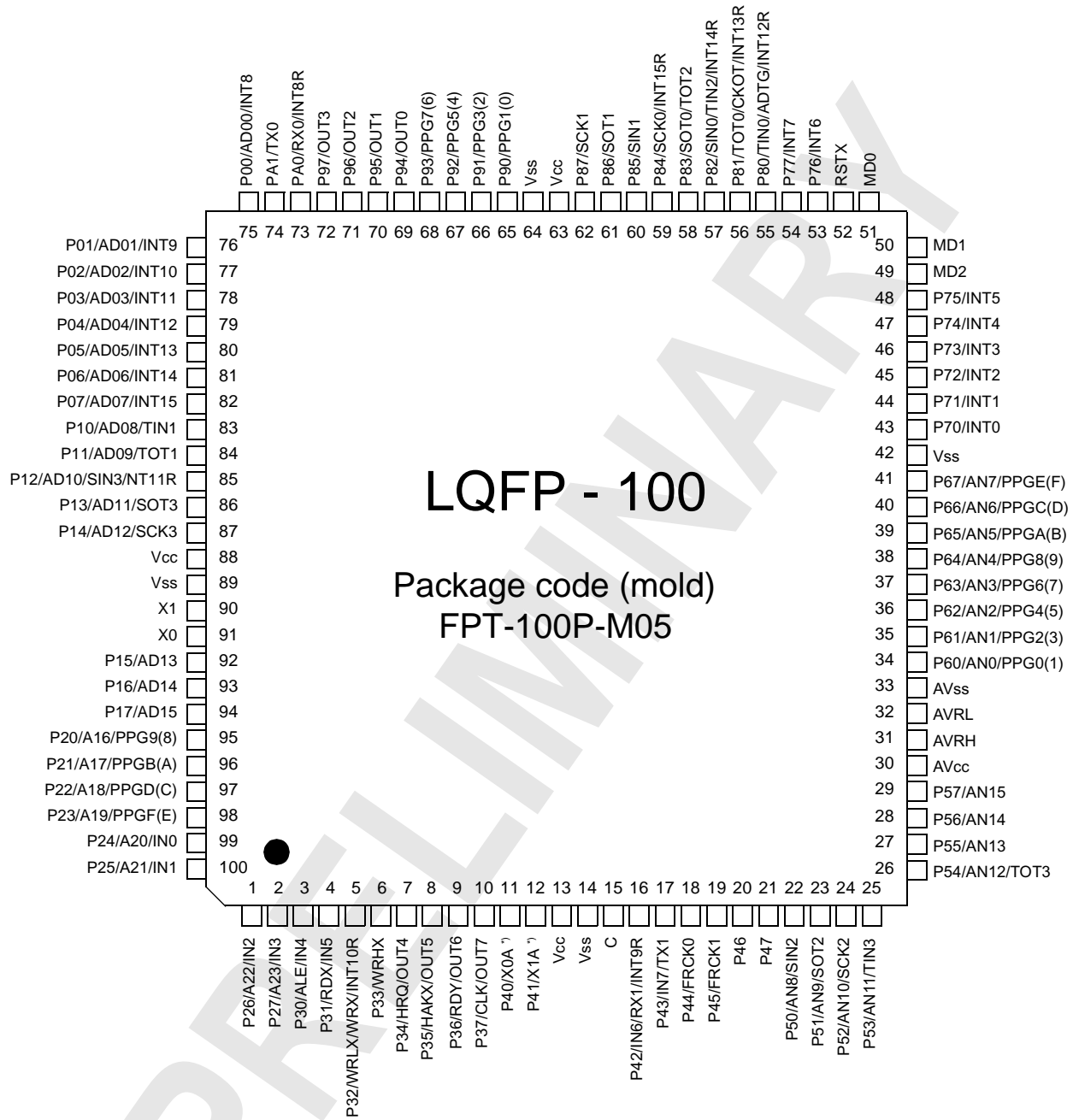
- MB90F342(S)/MB90F344(S)/MB90F347(S)
- MB90341(S)/MB90342(S)/MB90343(S)/MB90344(S)/MB90346(S)/MB90347(S)/MB90348(S)/MB90349(S)

(TOP VIEW)



\*) MB90F342/F344/F347/341/342/343/344/346/347/348/349 : X0A, X1A  
MB90F342S/F344S/F347S/341S/342S/343S/344S/346S/347S/348S/349S : P40, P41

(TOP VIEW)







# MB90340 Series

## ■ PIN DESCRIPTION

Pin No.		Pin name	Circuit type	Function
LQFP100 <sup>*2</sup>	QFP100 <sup>*1</sup>			
90	92	X1	A	Oscillation output
91	93	X0		Oscillation input
52	54	RSTX	E	Reset input
75 to 82	77 to 84	P00 to P07	G	General purpose IO
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins for INT8 to INT15.
83	85	P10	G	General purpose IO
		AD08		I/O pin for 8th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timers 1.
84	86	P11	G	General purpose IO
		AD09		I/O pin for 9th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer 1.
85	87	P12	N	General purpose IO
		AD10		I/O pin for 10th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3.
		INT11R		Second external interrupt request input pin for INT11.
86	88	P13	G	General purpose IO
		AD11		I/O pin for 11th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3.
87	89	P14	G	General purpose IO
		AD12		I/O pin for 12th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3.
92	94	P15	N	General purpose IO
		AD13		I/O pin for 13th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		SIN4		Serial data input pin for UART4 (MB90V340 only).

Pin No.		Pin name	Circuit type	Function
LQFP100 <sup>*2</sup>	QFP100 <sup>*1</sup>			
93	95	P16	G	General purpose IO
		AD14		I/O pin for 14th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		SOT4		Serial data output pin for UART4 (MB90V340 only).
94	96	P17	G	General purpose IO
		AD15		I/O pin for 15th bit of the external address/data bus. This function is enabled when the external bus is enabled.
		SCK4		Clock I/O pin for UART4 (MB90V340 only).
95 to 98	97 to 100	P20 to P23	G	General purpose IO
		A16 to A19		Output pins for A16 to A19 of the external address bus. This function is enabled when the external bus is enabled.
		PPG9,PPGB,PPGD,PPGF		Output pins for PPGs.
99 to 2	1 to 4	P24 to P27	G	General purpose IO
		A20 to A23		Output pins for A20 to A23 of the external address bus. This function is enabled when the external bus is enabled.
		IN0 to IN3		Data sample input pins for input captures ICU0 to ICU3.
3	5	P30	G	General purpose IO
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
		IN4		Data sample input pin for input capture ICU4.
4	6	P31	G	General purpose IO
		RDX		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
		IN5		Data sample input pin for input capture ICU5.
5	7	P32	G	General purpose IO
		WRLX / WRX		Write strobe output pin for the data bus. This function is enabled when both the external bus and the WR/WRL pin output are enabled. WRL is used to write-strobe 8 lower bits of the data bus in 16-bit access while WR is used to write-strobe 8 bits of the data bus in 8-bit access.
		RX2		RX input pin for CAN2 Interface (MB90V340 only).
		INT10R		Second external interrupt request input pin for INT10.

# MB90340 Series

Pin No.		Pin name	Circuit type	Function
LQFP100 <sup>*2</sup>	QFP100 <sup>*1</sup>			
6	8	P33	G	General purpose IO
		WRHX		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the WRH output pin is enabled.
		TX2		TX Output pin for CAN2 (MB90V340 only).
7	9	P34	G	General purpose IO
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compares OCU4. .
8	10	P35	G	General purpose IO
		HAKX		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compares OCU6.
9	11	P36	G	General purpose IO
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compares OCU5.
10	12	P37	G	General purpose IO
		CLK		CLK output pin. This function is enabled when both the external bus and CLK output are enabled.
		OUT7		Waveform output pin for output compares OCU7.
11 to 12	13 to 14	P40 to P41	F	General purpose IO (only for devices with S-suffix)
		X0A , X1A	B	Oscillator input pins for sub-clock (only for devices without S-suffix)
16	18	P42	F	General purpose IO
		IN6		Data sample input pin for input capture ICU6.
		RX1		RX input pin for CAN1 Interface (MB90F343/F344 only).
		INT9R		Second external interrupt request input pin for INT10.
17	19	P43	F	General purpose IO
		IN7		Data sample input pin for input capture ICU7.
		TX1		TX Output pin for CAN1 (MB90F343/F344 only).
18	20	P44	H	General purpose IO
		SDA0		Serial data I/O pin for I2C 0 (only devices with C-suffix)
		FRCK0		Input for the 16-bit IO Timer 0

Pin No.		Pin name	Circuit type	Function
LQFP100 <sup>*2</sup>	QFP100 <sup>*1</sup>			
19	21	P45	H	General purpose IO
		SCL0		Serial clock I/O pin for I2C 0 (only devices with C-suffix)
		FRCK1		Input for the 16-bit IO Timer 1
20	22	P46	H	General purpose IO
		SDA1		Serial data I/O pin for I2C 1 (only devices with C-suffix)
21	23	P47	H	General purpose IO
		SCL1		Serial clock I/O pin for I2C 1 (only devices with C-suffix)
22	24	P50	O	General purpose IO
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2.
23	25	P51	I	General purpose IO
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2.
24	26	P52	I	General purpose IO
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2.
25	27	P53	I	General purpose IO
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timers 3. .
26	28	P54	I	General purpose IO
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer 3.
27	29	P55	I	General purpose IO
		AN13		Analog input pin for the A/D converter
28 to 29	30 to 31	P56 to P57	J	General purpose IO
		AN14 to AN15		Analog input pin for the A/D converter
		DA00 to DA01		D/A converter analog output pins.
34 to 41	36 to 43	P60 to P67	I	General purpose IO
		AN0 to AN7		Analog input pins for the A/D converter.
		PPG0, 2, 4, 6, 8, A, C, E		Output pins for PPGs.

# MB90340 Series

Pin No.		Pin name	Circuit type	Function
LQFP100 <sup>2</sup>	QFP100 <sup>1</sup>			
43 to 48, 53, 54	45 to 50, 55, 56	P70 to P77	I	General purpose IO
		AN16 to AN23		Analog input pins for the A/D converter (only devices with C-suffix)
		INT0 to INT7		External interrupt request input pins for INT0 to INT7.
55	57	P80	F	General purpose IO
		TIN0		Event input pin for the reload timers 0.
		ADTG		Trigger input pin for the A/D converter.
		INT12R		Second external interrupt request input pin for INT12.
56	58	P81	F	General purpose IO
		TOT0		Output pin for the reload timer 0.
		CKOT		Output pin for the clock monitor.
		INT13R		Second external interrupt request input pin for INT13.
57	59	P82	M	General purpose IO
		SIN0		Serial data input pin for UART0.
		TIN2		Event input pin for the reload timers 2.
		INT14R		Second external interrupt request input pin for INT14.
58	60	P83	F	General purpose IO
		SOT0		Serial data output pin for UART0.
		TOT2		Output pin for the reload timer 2.
59	61	P84	F	General purpose IO
		SCK0		Clock I/O pin for UART0.
		INT15R		Second external interrupt request input pin for INT15.
60	62	P85	M	General purpose IO
		SIN1		Serial data input pin for UART1.
61	63	P86	F	General purpose IO
		SOT1		Serial data output pin for UART1.
62	64	P87	F	General purpose IO
		SCK1		Clock I/O pin for UART1.
65 to 68	67 to 70	P90 to P93	F	General purpose IO
		PPG1, 3, 5, 7		Output pins for PPGs.
69 to 72	71 to 74	P94 to P97	F	General purpose IO
		OUT0 to OUT3		Waveform output pins for output compares OCU0 to OCU3. This function is enabled when the OCU enables waveform output.

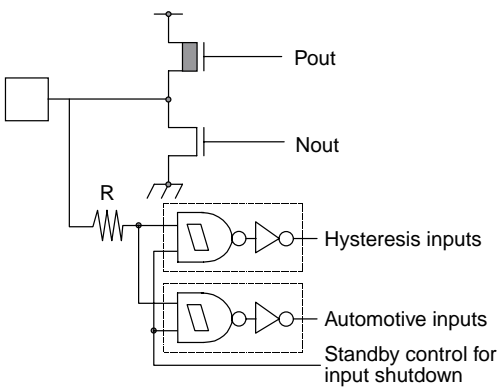
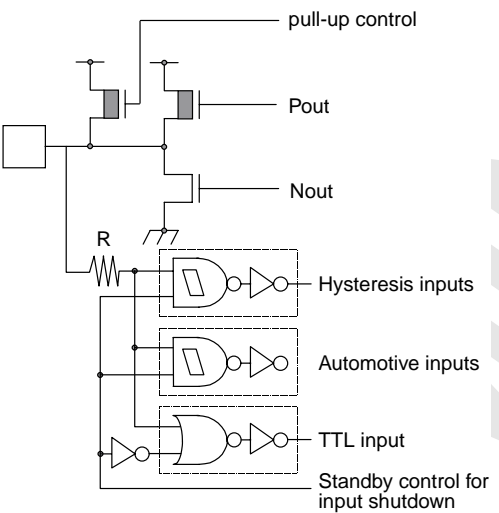
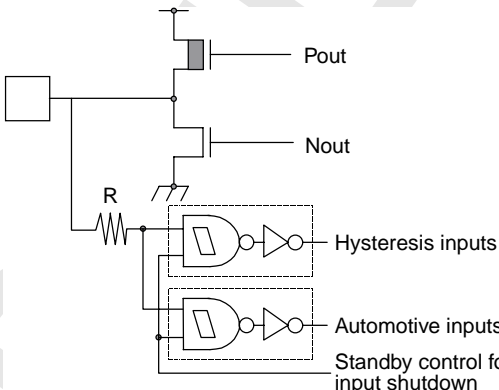
Pin No.		Pin name	Circuit type	Function
LQFP100 <sup>*2</sup>	QFP100 <sup>*1</sup>			
73	75	PA0	F	General purpose IO
		RX0		RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped.
		INT8R		Second external interrupt request input pin for INT8.
74	76	PA1	F	General purpose IO
		TX0		TX Output pin for CAN0.
30	32	AVCC	K	Vcc power input pin for analog circuits
31	33	AVRH	L	Reference voltage input for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV CC .
32	34	AVRL	K	Lower reference voltage input for the A/D Converter
33	35	AVSS	K	Vss power input pin for analog circuits
50 to 51	52 to 53	MD1 to MD0	C	Input pins for specifying the operating mode. The pins must be directly connected to Vcc or Vss
49	51	MD2	D	Input pin for specifying the operating mode. The pins must be directly connected to Vcc or Vss
14 63 88	15 65 90	VCC		Power (3.5V to 5.5V) input pins
14 42 64 89	16 44 66 91	VSS		Power (0V) input pins
15	17	C	K	This is the power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1μF ceramic capacitor.

\*1 : FPT-100P-M06

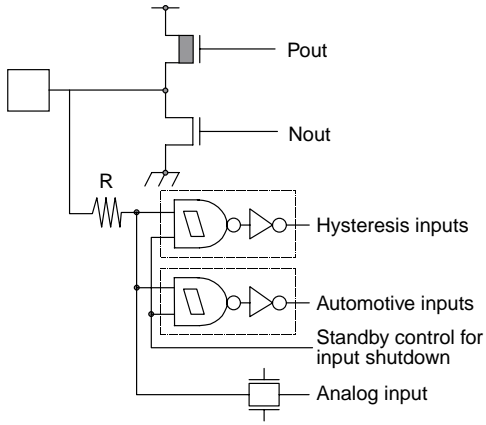
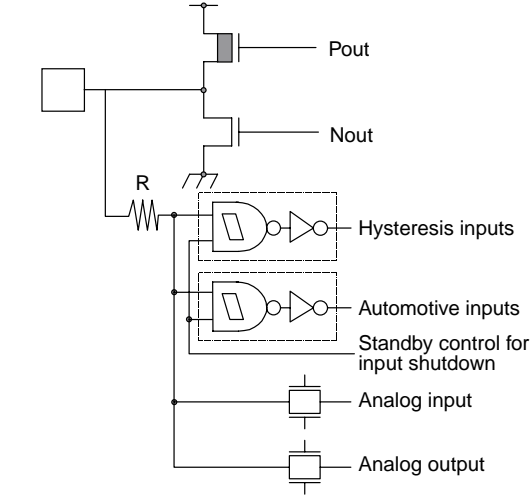
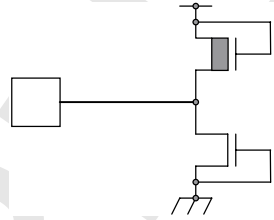
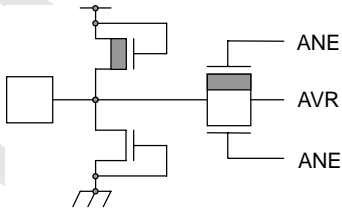
\*2 : FPT-100P-M05

## ■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<p>Oscillation circuit</p> <ul style="list-style-type: none"> <li>High-speed oscillation feedback resistor = approx. 1 MΩ</li> </ul>
B		<p>Oscillation circuit</p> <ul style="list-style-type: none"> <li>Low-speed oscillation feedback resistor = approx. 1 MΩ</li> </ul>
C		<p>Mask ROM and EVA device:</p> <ul style="list-style-type: none"> <li>CMOS Hysteresis input pin</li> <li>Resistor value : approx. 50 KΩ (TYP)</li> </ul> <p>Flash device:</p> <ul style="list-style-type: none"> <li>CMOS input pin</li> <li>Resistor value : approx. 50 KΩ (TYP)</li> </ul>
D		<p>Mask ROM and EVA device:</p> <ul style="list-style-type: none"> <li>CMOS Hysteresis input pin</li> <li>Resistor value : approx. 50 KΩ (TYP)</li> <li>Pull-down resistor value: approx. 50 kΩ</li> </ul> <p>Flash device:</p> <ul style="list-style-type: none"> <li>CMOS input pin</li> <li>Resistor value : approx. 50 KΩ (TYP)</li> <li>No Pull-down</li> </ul>
E		<p>CMOS Hysteresis input pin</p> <ul style="list-style-type: none"> <li>Resistor value : approx. 50 KΩ (TYP)</li> <li>Pull-up resistor value: approx. 50 kΩ</li> </ul>

Type	Circuit	Remarks
F	 <p>The diagram for Type F shows a CMOS output stage with a PMOS transistor (Pout) and an NMOS transistor (Nout). A pull-up resistor R is connected to the input of the PMOS transistor. The input signal is split to two input stages: Hysteresis inputs and Automotive inputs. A standby control block is also present, which can be used to shut down the input.</p>	<ul style="list-style-type: none"> <li>• CMOS level output(<math>I_{oL} = 4 \text{ mA}</math>)</li> <li>• CMOS hysteresis inputs (With the standby-time input shutdown function)</li> <li>• Automotive input (With the standby-time input shutdown function)</li> </ul>
G	 <p>The diagram for Type G shows a CMOS output stage with a PMOS transistor (Pout) and an NMOS transistor (Nout). A pull-up control input is connected to the PMOS transistor. A pull-up resistor R is connected to the input of the PMOS transistor. The input signal is split to three input stages: Hysteresis inputs, Automotive inputs, and TTL input. A standby control block is also present, which can be used to shut down the input.</p>	<ul style="list-style-type: none"> <li>• CMOS level output(<math>I_{oL} = 4 \text{ mA}</math>)</li> <li>• CMOS hysteresis inputs (With the standby-time input shutdown function)</li> <li>• Automotive input (With the standby-time input shutdown function)</li> <li>• TTL input (With the standby-time input shutdown function)</li> <li>• Programmable pullup resistor: <math>50\text{k}\Omega</math> approx.</li> </ul>
H	 <p>The diagram for Type H shows a CMOS output stage with a PMOS transistor (Pout) and an NMOS transistor (Nout). A pull-up resistor R is connected to the input of the PMOS transistor. The input signal is split to two input stages: Hysteresis inputs and Automotive inputs. A standby control block is also present, which can be used to shut down the input.</p>	<ul style="list-style-type: none"> <li>• CMOS level output(<math>I_{oL} = 3 \text{ mA}</math>)</li> <li>• CMOS hysteresis inputs (With the standby-time input shutdown function)</li> <li>• Automotive input (With the standby-time input shutdown function)</li> </ul>

# MB90340 Series

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> <li>• CMOS level output(<math>I_{OL} = 4 \text{ mA}</math>)</li> <li>• CMOS hysteresis inputs (With the standby-time input shutdown function)</li> <li>• Automotive input (With the standby-time input shutdown function)</li> <li>• A/D analog input</li> </ul>
J		<ul style="list-style-type: none"> <li>• CMOS level output(<math>I_{OL} = 4 \text{ mA}</math>)</li> <li>• D/A analog output</li> <li>• CMOS hysteresis inputs (With the standby-time input shutdown function)</li> <li>• Automotive input (With the standby-time input shutdown function)</li> <li>• A/D analog input</li> </ul>
K		<p>Power supply input protection circuit</p> <ul style="list-style-type: none"> <li>• Flash devices do not have a protection circuit against VCC for pin AVRH</li> </ul>
L		<ul style="list-style-type: none"> <li>• A/D converter ref+ (AVRH) power supply input pin, With the protection circuit</li> </ul>



## ■ HANDLING DEVICES

Special care is required for the following when handling the device :

- Preventing latch-up
- Treatment of unused pins
- Using external clock
- Power supply pins ( $V_{CC}/V_{SS}$ )
- Pull-up/down resistors
- Crystal Oscillator Circuit
- Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter
- Notes on Energization
- Initialization
- Port0 to port3 output during Power-on(**External-bus mode**)

### 1. Preventing latch-up

**CMOS IC chips may suffer latch-up under the following conditions :**

- A voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between  $V_{CC}$  and  $V_{SS}$ .
- The  $AV_{CC}$  power supply is applied before the  $V_{CC}$  voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage ( $AV_{CC}$ ,  $AVRH$ ) exceed the digital power-supply voltage.

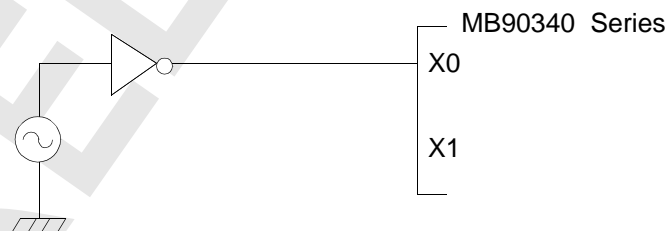
### 2. Handling unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 K $\Omega$  .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

### 3. Using external clock

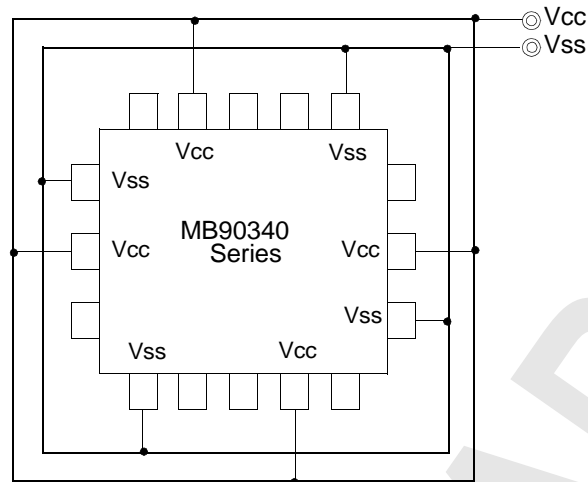
To use external clock, drive the X0 pin and leave X1 pin open.



### 4. Power supply pins ( $V_{CC}/V_{SS}$ )

- If there are multiple  $V_{CC}$  and  $V_{SS}$  pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.  
To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the  $V_{CC}$  and  $V_{SS}$  pins to the power supply and ground externally.
- Connect  $V_{CC}$  and  $V_{SS}$  to the device from the current supply source at a low impedance.

- As a measure against power supply noise, connect a capacitor of about 0.1  $\mu\text{F}$  as a bypass capacitor between  $V_{\text{CC}}$  and  $V_{\text{SS}}$  in the vicinity of  $V_{\text{CC}}$  and  $V_{\text{SS}}$  pins of the device



## 5. Pull-up/down resistors

The MB90340 Series does not support internal pull-up/down resistors (except Port0 - Port3: programmable pull-up resistors). Use external components where needed.

## 6. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

## 7. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply ( $AV_{\text{CC}}$ ,  $AV_{\text{RH}}$ ,  $AV_{\text{RL}}$ ) and analog inputs (AN0 to AN14) after turning-on the digital power supply ( $V_{\text{CC}}$ ).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage not exceed  $AV_{\text{RH}}$  or  $AV_{\text{CC}}$  (turning on/off the analog and digital power supplies simultaneously is acceptable).

## 8. Connection of Unused Pins of A/D Converter if A/D Converter is used

Connect unused pins of A/D converter to  $AV_{\text{CC}} = V_{\text{CC}}$ ,  $AV_{\text{SS}} = AV_{\text{RH}} = AV_{\text{RL}} = V_{\text{SS}}$ .

## 9. Notes on Energization

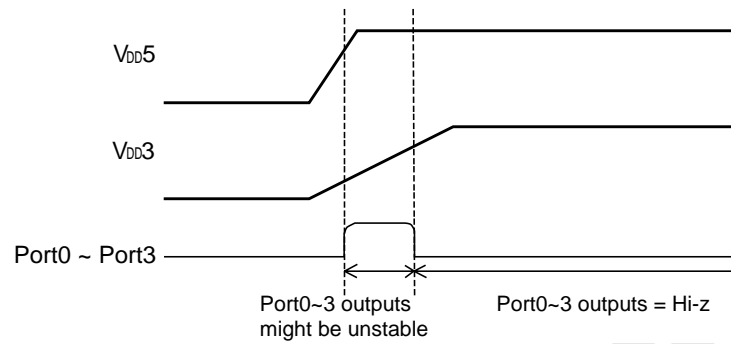
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 or more  $\mu\text{s}$  (0.2 V to 2.7 V)

## 10. Initialization

In the device, there are internal registers which is initialized only by a power-on reset. To initialize these registers, turn on the power again.

## 11. Port0 to 3 output during Power-on (External-bus mode)

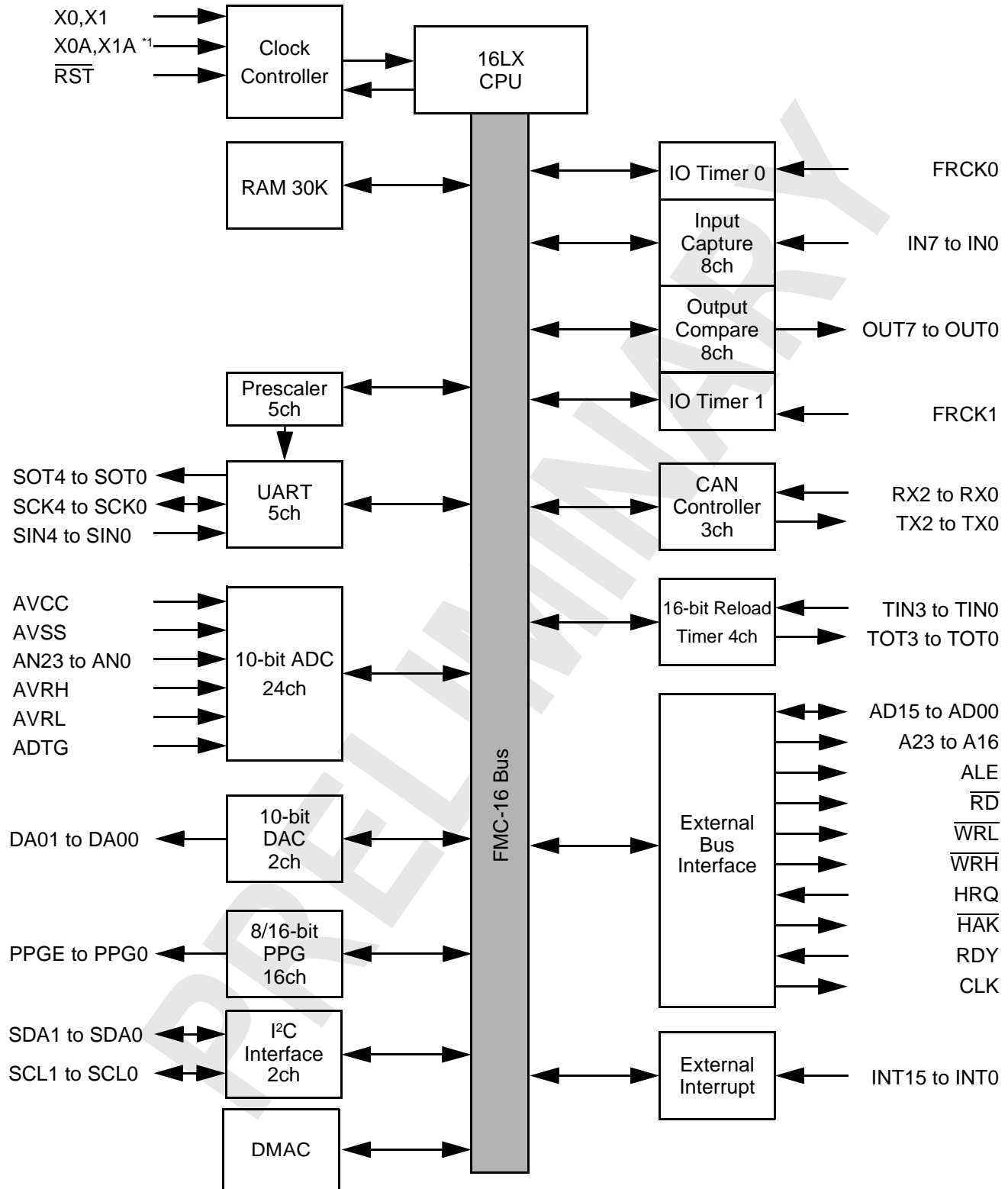
As shown below, when power is turned on in External-Bus mode, there is a possibility that output signal of Port0 to Port3 might be unstable.



PRELIMINARY

## ■ BLOCK DIAGRAMS

### MB90V340(S)

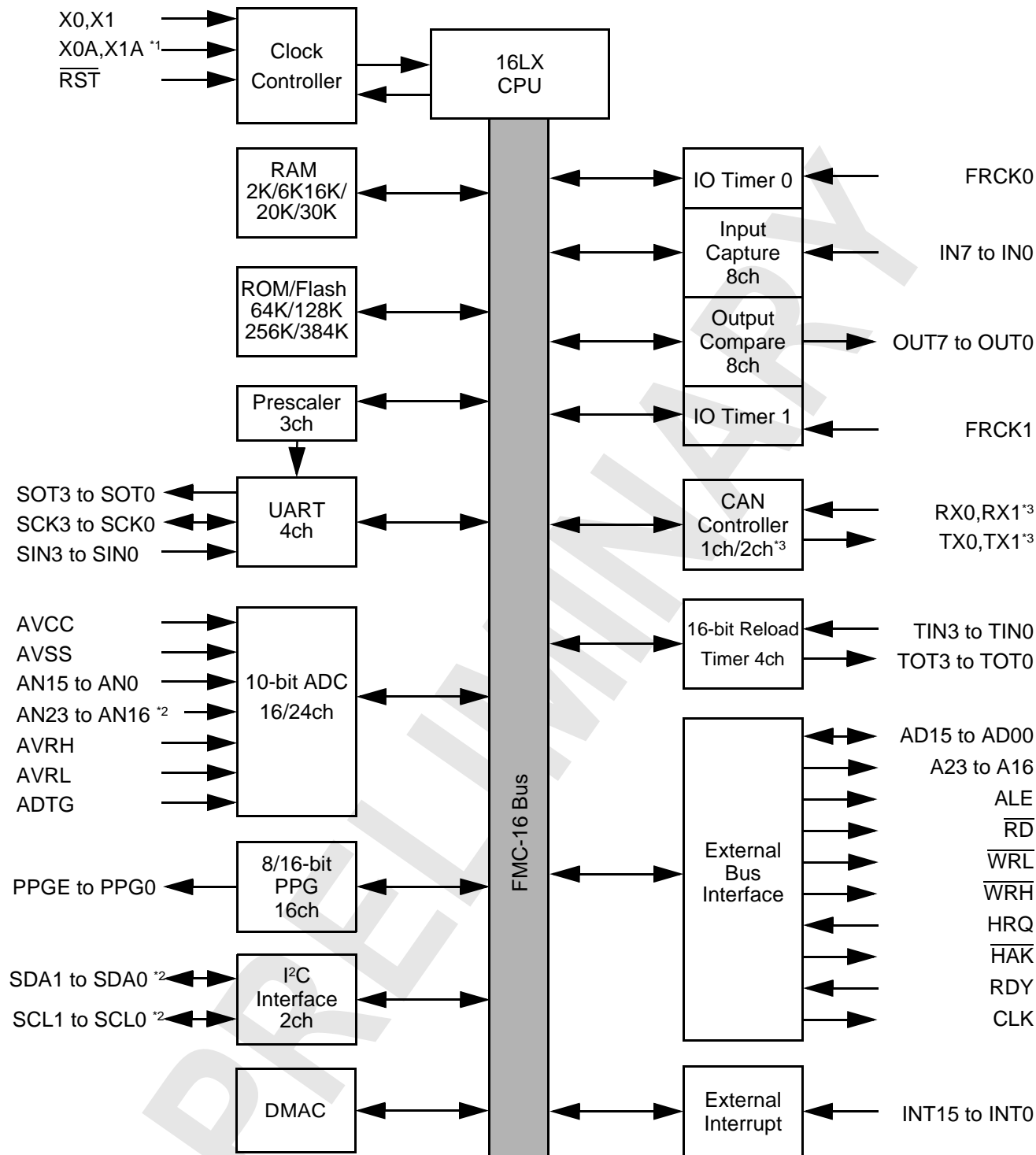


\*1) Only for MB90V340 ( without 'S' Suffix )

# MB90340 Series

MB90F342/C(S), MB90F344/C(S), MB90F347/C(S)

MB90341/C(S), MB90342/C(S), MB90343/C(S), MB90344/C(S), MB90346/C(S), MB90347/C(S), MB90348/C(S), MB90349/C(S)




\*1) Only for devices without 'S' Suffix

\*2) Only for devices with 'C' Suffix

\*3) Only for devices with 'C' Suffix

## ■ MEMORY SPACE

MB90V340	MB90344/C/S/CS MB90F344/C/S/CS	MB90F343/C/S/CS
FFFFFFH ROM (FF bank)	FFFFFFH ROM (FF bank)	FFFFFFH ROM (FF bank)
FF0000H ROM (FE bank)	FF0000H ROM (FE bank)	FF0000H ROM (FE bank)
FE0000H ROM (FD bank)	FE0000H ROM (FD bank)	FE0000H ROM (FD bank)
FDF000H ROM (FC bank)	FDF000H ROM (FC bank)	FDF000H ROM (FC bank)
FD0000H ROM (FB bank)	FD0000H ROM (FB bank)	FD0000H ROM (FB bank)
FC0000H ROM (FA bank)	FC0000H ROM (FA bank)	FC0000H ROM (FA bank)
FB0000H ROM (F9 bank)	FB0000H ROM (F9 bank)	FB0000H ROM (F9 bank)
F90000H	F90000H	F90000H
00FFFFFFH ROM (Image of FF bank)	00FFFFFFH ROM (Image of FF bank)	00FFFFFFH ROM (Image of FF bank)
008000H Peripheral	008000H Peripheral	008000H Peripheral
007FFFH	007FFFH	007FFFH
007900H	007900H	007900H
0078FFH	0078FFH	0078FFH
		0050FFH
		RAM 20K
000100H	000100H	000100H
0000EFH Peripheral	0000EFH Peripheral	0000EFH Peripheral
000000H	000000H	000000H

 :No access



## ■ I/O MAP

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
00 <sub>H</sub>	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX
01 <sub>H</sub>	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX
02 <sub>H</sub>	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX
03 <sub>H</sub>	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX
04 <sub>H</sub>	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX
05 <sub>H</sub>	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX
06 <sub>H</sub>	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX
07 <sub>H</sub>	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXX
08 <sub>H</sub>	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX
09 <sub>H</sub>	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX
0A <sub>H</sub>	Port A data register	PDRA	R/W	Port A	XXXXXXXX
0B <sub>H</sub>	Analog Input Enable Port 5	ADER5	R/W	Port 5, A/D	11111111
0C <sub>H</sub>	Analog Input Enable Port 6	ADER6	R/W	Port 6, A/D	11111111
0D <sub>H</sub>	Analog Input Enable Port 7	ADER7	R/W	Port 7, A/D	11111111
0E <sub>H</sub>	Input level select register0	ILSR0	R/W	Ports	XXXXXXXX
0F <sub>H</sub>	Input level select register1	ILSR1	R/W	Ports	XXXXXXXX
10 <sub>H</sub>	Port 0 direction register	DDR0	R/W	Port 0	00000000
11 <sub>H</sub>	Port 1 direction register	DDR1	R/W	Port 1	00000000
12 <sub>H</sub>	Port 2 direction register	DDR2	R/W	Port 2	00000000
13 <sub>H</sub>	Port 3 direction register	DDR3	R/W	Port 3	00000000
14 <sub>H</sub>	Port 4 direction register	DDR4	R/W	Port 4	00000000
15 <sub>H</sub>	Port 5 direction register	DDR5	R/W	Port 5	00000000
16 <sub>H</sub>	Port 6 direction register	DDR6	R/W	Port 6	00000000
17 <sub>H</sub>	Port 7 direction register	DDR7	R/W	Port 7	00000000
18 <sub>H</sub>	Port 8 direction register	DDR8	R/W	Port 8	00000000
19 <sub>H</sub>	Port 9 direction register	DDR9	R/W	Port 9	00000000
1A <sub>H</sub>	Port A direction register	DDRA	R/W	Port A	00000100
1B <sub>H</sub>	Reserved				
1C <sub>H</sub>	Port 0 Pullup control register	PUCR0	R/W	Port 0	00000000
1D <sub>H</sub>	Port 1 Pullup control register	PUCR1	R/W	Port 1	00000000
1E <sub>H</sub>	Port 2 Pullup control register	PUCR2	R/W	Port 2	00000000
1F <sub>H</sub>	Port 3 Pullup control register	PUCR3	W, R/W	Port 3	00000000

# MB90340 Series

Address	Register	Abbreviation	Access	Resource name	Initial value
20H	Serial Mode Register	SMR0	W,R/W	UART0	00000000
21H	Serial Control Register	SCR0	W,R/W		00000000
22H	Reception/Transmission Data Register	RDR0/ TDR0	R/W		00000000
23H	Serial Status Register	SSR0	R,R/W		00001000
24H	Extended Communication Control Reg.	ECCR0	R,W,R/W		000000XX
25H	Extended Status/Control Register	ESCR0	R/W		00000100
26H	Baud Rate Register 0	BGR00	R/W		00000000
27H	Baud Rate Register 1	BGR01	R/W	00000000	
28H	Serial Mode Register	SMR1	W,R/W	UART1	00000000
29H	Serial Control Register	SCR1	W,R/W		00000000
2AH	Reception/Transmission Data Register	RDR1/ TDR1	R/W		00000000
2BH	Serial Status Register	SSR1	R,R/W		00001000
2CH	Extended Communication Control Reg.	ECCR1	R,W,R/W		000000XX
2DH	Extended Status/Control Register	ESCR1	R/W		00000100
2EH	Baud Rate Register 0	BGR10	R/W		00000000
2FH	Baud Rate Register 1	BGR11	R/W	00000000	
30H	PPG0 operation mode control register	PPGC0	W,R/W	16-bit Programmable Pulse Generator 0/1	0X000XX1
31H	PPG1 operation mode control register	PPGC1	W,R/W		0X000001
32H	PPG0 and PPG1 clock select register	PPG01	R/W		000000X0
33H	Reserved				
34H	PPG2 operation mode control register	PPGC2	W,R/W	16-bit Programmable Pulse Generator 2/3	0X000XX1
35H	PPG3 operation mode control register	PPGC3	W,R/W		0X000001
36H	PPG2 and PPG3 clock select register	PPG23	R/W		000000X0
37H	Reserved				
38H	PPG4 operation mode control register	PPGC4	W,R/W	16-bit Programmable Pulse Generator 4/5	0X000XX1
39H	PPG5 operation mode control register	PPGC5	W,R/W		0X000001
3AH	PPG4 and PPG5 clock select register	PPG45	R/W		000000X0
3BH	ROM Correction Control Status 1	PACSR1	R/W	ROM Correction 1	00000000
3CH	PPG6 operation mode control register	PPGC6	W,R/W	16-bit Programmable Pulse Generator 6/7	0X000XX1
3DH	PPG7 operation mode control register	PPGC7	W,R/W		0X000001
3EH	PPG6 and PPG7 clock select register	PPG67	R/W		000000X0
3FH	Reserved				
40H	PPG8 operation mode control register	PPGC8	W,R/W	16-bit Programmable Pulse Generator 8/9	0X000XX1
41H	PPG9 operation mode control register	PPGC9	W,R/W		0X000001
42H	PPG8 and PPG9 clock select register	PPG89	R/W		000000X0

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
43H	Reserved				
44H	PPGA operation mode control register	PPGCA	W,R/W	16-bit Programmable Pulse Generator A/B	0X000XX1
45H	PPGB operation mode control register	PPGCB	W,R/W		0X000001
46H	PPGA and PPGB clock select register	PPGAB	R/W		000000X0
47H	Reserved				
48H	PPGC operation mode control register	PPGCC	W,R/W	16-bit Programmable Pulse Generator C/D	0X000XX1
49H	PPGD operation mode control register	PPGCD	W,R/W		0X000001
4AH	PPGC and PPGD clock select register	PPGCD	R/W		000000X0
4BH	Reserved				
4CH	PPGE operation mode control register	PPGCE	W,R/W	16-bit Programmable Pulse Generator E/F	0X000XX1
4DH	PPGF operation mode control register	PPGCF	W,R/W		0X000001
4EH	PPGE and PPGF clock select register	PPGEF	R/W		000000X0
4FH	Reserved				
50H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000
51H	Input Capture Edge 0/1	ICE01	R/W		XXX0X0XX
52H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000
53H	Input Capture Edge 2/3	ICE23	R/W		XXXXXXXXXX
54H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000
55H	Input Capture Edge 4/5	ICE45	R/W		XXXXXXXXXX
56H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000
57H	Input Capture Edge 6/7	ICE67	R/W		XXX000XX
58H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00
59H	Output Compare Control Status 1	OCS1	R/W		0XX00000
5AH	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00
5BH	Output Compare Control Status 3	OCS3	R/W		0XX00000
5CH	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	0000XX00
5DH	Output Compare Control Status 5	OCS5	R/W		0XX00000
5EH	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	0000XX00
5FH	Output Compare Control Status 7	OCS7	R/W		0XX00000
60H	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000
61H	Timer Control Status 0	TMCSR0	R/W		XXXX0000
62H	Timer Control Status 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000
63H	Timer Control Status 1	TMCSR1	R/W		XXXX0000
64H	Timer Control Status 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000
65H	Timer Control Status 2	TMCSR2	R/W		XXXX0000

# MB90340 Series

Address	Register	Abbreviation	Access	Resource name	Initial value
66H	Timer Control Status 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000
67H	Timer Control Status 3	TMCSR3	R/W		XXXX0000
68H	A/D Control Status 0	ADCS0	R/W	A/D Converter	000XXXX0
69H	A/D Control Status 1	ADCS1	R/W		0000000X
6AH	A/D Data 0	ADCR0	R		00000000
6BH	A/D Data 1	ADCR1	R		XXXXXX00
6CH	ADC Setting 0	ADSR0	R/W		00000000
6D	ADC Setting 1	ADSR1	R/W		00000000
6EH	Reserved				
6FH	ROM Mirror	ROMM	W	ROM Mirror	XXXXXXXX1
70 to 8FH	Reserved for CAN Interface 0/1. Refer to "■ CAN CONTROLLERS"				
90 to 9AH	Reserved				
9BH	DMA Descriptor Channel Select	DCSR	R/W	DMA	00000000
9CH	DMA Status L	DSRL	R/W		00000000
9DH	DMA Status H	DSRH	R/W		00000000
9EH	ROM Correction Control Status 0	PACSR0	R/W	ROM Correction 0	00000000
9FH	Delayed Interrupt/release	DIRR	R/W	Delayed Interrupt	XXXXXXXX0
A0H	Low-power Mode Control	LPMCR	W,R/W	Low Power Controller	00011000
A1H	Clock Selection	CKSCR	R,R/W	Low Power Controller	11111100
A2 to A3H	Reserved				
A4H	DMA Stop Status	DSSR	R/W	DMA	00000000
A5H	Automatic ready function select reg.	ARSR	W	External Memory Access	0011XX00
A6H	External address output control reg.	HACR	W		00000000
A7H	Bus control signal selection register	ECSR	W		0000000X
A8H	Watchdog Control	WDTC	R,W	Watchdog Timer	XXXXX111
A9H	Time Base Timer Control	TBTC	W,R/W	Time Base Timer	1XX00100
AAH	Watch Timer Control register	WTC	R,R/W	Watch Timer	1X001000
ABH	Reserved				
ACH	DMA Enable L	DERL	R/W	DMA	00000000
ADH	DMA Enable H	DERH	R/W		00000000
AEH	Flash Control Status (FlashDevices only.Otherwise reserved)	FMCS	R,R/W	Flash Memory	000X0000
AFH	Reserved				

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
B0 <sub>H</sub>	Interrupt control register 00	ICR00	W,R/W	Interrupt controller	00000111
B1 <sub>H</sub>	Interrupt control register 01	ICR01	W,R/W		00000111
B2 <sub>H</sub>	Interrupt control register 02	ICR02	W,R/W		00000111
B3 <sub>H</sub>	Interrupt control register 03	ICR03	W,R/W		00000111
B4 <sub>H</sub>	Interrupt control register 04	ICR04	W,R/W		00000111
B5 <sub>H</sub>	Interrupt control register 05	ICR05	W,R/W		00000111
B6 <sub>H</sub>	Interrupt control register 06	ICR06	W,R/W		00000111
B7 <sub>H</sub>	Interrupt control register 07	ICR07	W,R/W		00000111
B8 <sub>H</sub>	Interrupt control register 08	ICR08	W,R/W		00000111
B9 <sub>H</sub>	Interrupt control register 09	ICR09	W,R/W		00000111
BA <sub>H</sub>	Interrupt control register 10	ICR10	W,R/W		00000111
BB <sub>H</sub>	Interrupt control register 11	ICR11	W,R/W		00000111
BC <sub>H</sub>	Interrupt control register 12	ICR12	W,R/W		00000111
BD <sub>H</sub>	Interrupt control register 13	ICR13	W,R/W		00000111
BE <sub>H</sub>	Interrupt control register 14	ICR14	W,R/W		00000111
BF <sub>H</sub>	Interrupt control register 15	ICR15	W,R/W		00000111
C0 <sub>H</sub>	D/A Converter data 0	DAT0	R/W	D/A Converter	XXXXXXXX
C1 <sub>H</sub>	D/A Converter data 1	DAT1	R/W		XXXXXXXX
C2 <sub>H</sub>	D/A Control 0	DACR0	R/W		XXXXXXXX0
C3 <sub>H</sub>	D/A Control 1	DACR1	R/W		XXXXXXXX0
C4 to C5 <sub>H</sub>	Reserved				
C6 <sub>H</sub>	External Interrupt Enable 0	ENIR0	R/W	External Interrupt 0	00000000
C7 <sub>H</sub>	External Interrupt Request 0	EIRR0	R/W		XXXXXXXX
C8 <sub>H</sub>	External Interrupt Level 0	ELVR0	R/W		00000000
C9 <sub>H</sub>	External Interrupt Level 0	ELVR0	R/W		00000000
CA <sub>H</sub>	External Interrupt Enable 1	ENIR1	R/W	External Interrupt 1	00000000
CB <sub>H</sub>	External Interrupt Request 1	EIRR1	R/W		XXXXXXXX
CC <sub>H</sub>	External Interrupt Level 1	ELVR1	R/W		00000000
CD <sub>H</sub>	External Interrupt Level 1	ELVR1	R/W		00000000
CE <sub>H</sub>	External Interrupt 1 Source Select	EISSR	R/W		00000000
CF <sub>H</sub>	PLL/Subclock Control register	PSCCR	W	PLL	XXXX0000

# MB90340 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
D0 <sub>H</sub>	DMA Buffer Addrss Pointer L	BAPL	R/W	DMA	XXXXXXXX
D1 <sub>H</sub>	DMA Buffer Addrss Pointer M	BAPM	R/W		XXXXXXXX
D2 <sub>H</sub>	DMA Buffer Addrss Pointer H	BAPH	R/W		XXXXXXXX
D3 <sub>H</sub>	DMA Control	DMACS	R/W		XXXXXXXX
D4 <sub>H</sub>	I/O Register Address Pointer L	IOAL	R/W		XXXXXXXX
D5 <sub>H</sub>	I/O Register Address Pointer H	IOAH	R/W		XXXXXXXX
D6 <sub>H</sub>	Data Counter L	DCTL	R/W		XXXXXXXX
D7 <sub>H</sub>	Data Counter H	DCTH	R/W		XXXXXXXX
D8 <sub>H</sub>	Serial Mode Register	SMR2	W,R/W	UART2	00000000
D9 <sub>H</sub>	Serial Control Register	SCR2	W,R/W		00000000
DA <sub>H</sub>	Reception/Transmission Data Register	RDR2/ TDR2	R/W		00000000
DB <sub>H</sub>	Serial Status Register	SSR2	R,R/W		00001000
DC <sub>H</sub>	Extended Communication Control Reg.	ECCR2	R,W,R/W		000000XX
DD <sub>H</sub>	Extended Status/Control Register	ESCR2	R/W		00000100
DE <sub>H</sub>	Baud Rate Register 0	BGR20	R/W		00000000
DF <sub>H</sub>	Baud Rate Register 1	BGR21	R/W		00000000
E0 to EF <sub>H</sub>	Reserved for CAN Interface 2. Refer to "■ CAN CONTROLLERS"				
FO to FF <sub>H</sub>	External				

(Continued)

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
7900 <sub>H</sub>	Reload L	PRLLO	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX
7901 <sub>H</sub>	Reload H	PRLH0	R/W		XXXXXXXX
7902 <sub>H</sub>	Reload L	PRL11	R/W		XXXXXXXX
7903 <sub>H</sub>	Reload H	PRLH1	R/W		XXXXXXXX
7904 <sub>H</sub>	Reload L	PRL22	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX
7905 <sub>H</sub>	Reload H	PRLH2	R/W		XXXXXXXX
7906 <sub>H</sub>	Reload L	PRL33	R/W		XXXXXXXX
7907 <sub>H</sub>	Reload H	PRLH3	R/W		XXXXXXXX
7908 <sub>H</sub>	Reload L	PRL44	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX
7909 <sub>H</sub>	Reload H	PRLH4	R/W		XXXXXXXX
790A <sub>H</sub>	Reload L	PRL55	R/W		XXXXXXXX
790B <sub>H</sub>	Reload H	PRLH5	R/W		XXXXXXXX
790C <sub>H</sub>	Reload L	PRL66	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX
790D <sub>H</sub>	Reload H	PRLH6	R/W		XXXXXXXX
790E <sub>H</sub>	Reload L	PRL77	R/W		XXXXXXXX
790F <sub>H</sub>	Reload H	PRLH7	R/W		XXXXXXXX
7910 <sub>H</sub>	Reload L	PRL88	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXX
7911 <sub>H</sub>	Reload H	PRLH8	R/W		XXXXXXXX
7912 <sub>H</sub>	Reload L	PRL99	R/W		XXXXXXXX
7913 <sub>H</sub>	Reload H	PRLH9	R/W		XXXXXXXX
7914 <sub>H</sub>	Reload L	PRLLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXX
7915 <sub>H</sub>	Reload H	PRLHA	R/W		XXXXXXXX
7916 <sub>H</sub>	Reload L	PRLLB	R/W		XXXXXXXX
7917 <sub>H</sub>	Reload H	PRLHB	R/W		XXXXXXXX
7918 <sub>H</sub>	Reload L	PRLLC	R/W	16-bit Programmable Pulse Generator C/D	XXXXXXXX
7919 <sub>H</sub>	Reload H	PRLHC	R/W		XXXXXXXX
791A <sub>H</sub>	Reload L	PRLLD	R/W		XXXXXXXX
791B <sub>H</sub>	Reload H	PRLHD	R/W		XXXXXXXX
791C <sub>H</sub>	Reload L	PRLLE	R/W	16-bit Programmable Pulse Generator E/F	XXXXXXXX
791D <sub>H</sub>	Reload H	PRLHE	R/W		XXXXXXXX
791E <sub>H</sub>	Reload L	PRLLF	R/W		XXXXXXXX
791F <sub>H</sub>	Reload H	PRLHF	R/W		XXXXXXXX
7920 <sub>H</sub>	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX
7921 <sub>H</sub>	Input Capture 0	IPCP0	R		XXXXXXXX
7922 <sub>H</sub>	Input Capture 1	IPCP1	R		XXXXXXXX
7923 <sub>H</sub>	Input Capture 1	IPCP1	R		XXXXXXXX

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Address	Register	Abbrevia- tion	Access	Resource name	Initial value
7924 <sub>H</sub>	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX
7925 <sub>H</sub>	Input Capture 2	IPCP2	R		XXXXXXXX
7926 <sub>H</sub>	Input Capture 3	IPCP3	R		XXXXXXXX
7927 <sub>H</sub>	Input Capture 3	IPCP3	R		XXXXXXXX
7928 <sub>H</sub>	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX
7929 <sub>H</sub>	Input Capture 4	IPCP4	R		XXXXXXXX
792A <sub>H</sub>	Input Capture 5	IPCP5	R		XXXXXXXX
792B <sub>H</sub>	Input Capture 5	IPCP5	R		XXXXXXXX
792C <sub>H</sub>	Input Capture 6	IPCP6	R	Input Capture 6/7	XXXXXXXX
792D <sub>H</sub>	Input Capture 6	IPCP6	R		XXXXXXXX
792E <sub>H</sub>	Input Capture 7	IPCP7	R		XXXXXXXX
792F <sub>H</sub>	Input Capture 7	IPCP7	R		XXXXXXXX
7930 <sub>H</sub>	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX
7931 <sub>H</sub>	Output Compare 0	OCCP0	R/W		XXXXXXXX
7932 <sub>H</sub>	Output Compare 1	OCCP1	R/W		XXXXXXXX
7933 <sub>H</sub>	Output Compare 1	OCCP1	R/W		XXXXXXXX
7934 <sub>H</sub>	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX
7935 <sub>H</sub>	Output Compare 2	OCCP2	R/W		XXXXXXXX
7936 <sub>H</sub>	Output Compare 3	OCCP3	R/W		XXXXXXXX
7937 <sub>H</sub>	Output Compare 3	OCCP3	R/W		XXXXXXXX
7938 <sub>H</sub>	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX
7939 <sub>H</sub>	Output Compare 4	OCCP4	R/W		XXXXXXXX
793A <sub>H</sub>	Output Compare 5	OCCP5	R/W		XXXXXXXX
793B <sub>H</sub>	Output Compare 5	OCCP5	R/W		XXXXXXXX
793C <sub>H</sub>	Output Compare 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX
793D <sub>H</sub>	Output Compare 6	OCCP6	R/W		XXXXXXXX
793E <sub>H</sub>	Output Compare 7	OCCP7	R/W		XXXXXXXX
793F <sub>H</sub>	Output Compare 7	OCCP7	R/W		XXXXXXXX
7940 <sub>H</sub>	Timer Data 0	TCDT0	R/W	I/O Timer 0	00000000
7941 <sub>H</sub>	Timer Data 0	TCDT0	R/W		00000000
7942 <sub>H</sub>	Timer Control 0	TCCSL0	R/W		00000000
7943 <sub>H</sub>	Timer Control 0	TCCSH0	R/W		0XXXXXXXX
7944 <sub>H</sub>	Timer Data 1	TCDT1	R/W	I/O Timer 1	00000000
7945 <sub>H</sub>	Timer Data 1	TCDT1	R/W		00000000
7946 <sub>H</sub>	Timer Control 1	TCCSL1	R/W		00000000
7947 <sub>H</sub>	Timer Control 1	TCCSH1	R/W		0XXXXXXXX

Address	Register	Abbrevia- tion	Access	Resource name	Initial value	
7948 <sub>H</sub>	Timer 0/Reload 0	TMR0/ TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX	
7949 <sub>H</sub>			R/W		XXXXXXXX	
794A <sub>H</sub>	Timer 1/Reload 1	TMR1/ TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX	
794B <sub>H</sub>			R/W		XXXXXXXX	
794C <sub>H</sub>	Timer 2/Reload 2	TMR2/ TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXX	
794D <sub>H</sub>			R/W		XXXXXXXX	
794E <sub>H</sub>	Timer 3/Reload 3	TMR3/ TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXX	
794F <sub>H</sub>			R/W		XXXXXXXX	
7950 <sub>H</sub>	Serial Mode Register	SMR3	W,R/W	UART3	00000000	
7951 <sub>H</sub>	Serial Control Register	SCR3	W,R/W		00000000	
7952 <sub>H</sub>	Reception/Transmission Data Register	RDR3/ TDR3	R/W		00000000	
7953 <sub>H</sub>	Serial Status Register	SSR3	R,R/W		00001000	
7954 <sub>H</sub>	Extended Communication Control Reg.	ECCR3	R,W,R/W		000000XX	
7955 <sub>H</sub>	Extended Status/Control Register	ESCR3	R/W		00000100	
7956 <sub>H</sub>	Baud Rate Register 0	BGR30	R/W		00000000	
7957 <sub>H</sub>	Baud Rate Register 1	BGR31	R/W		00000000	
7958 <sub>H</sub>	Serial Mode Register	SMR4	W,R/W		UART4	00000000
7959 <sub>H</sub>	Serial Control Register	SCR4	W,R/W			00000000
795A <sub>H</sub>	Reception/Transmission Data Register	RDR4/ TDR4	R/W	00000000		
795B <sub>H</sub>	Serial Status Register	SSR4	R,R/W	00001000		
795C <sub>H</sub>	Extended Communication Control Reg.	ECCR4	R,W,R/W	000000XX		
795D <sub>H</sub>	Extended Status/Control Register	ESCR4	R/W	00000100		
795E <sub>H</sub>	Baud Rate Register 0	BGR40	R/W	00000000		
795F <sub>H</sub>	Baud Rate Register 1	BGR41	R/W	00000000		
7960 to 796B <sub>H</sub>	Reserved					
796C <sub>H</sub>	Clock output enable register	CLKR	R/W	Clock Monitor	XXXX0000	
796D <sub>H</sub>	Reserved					
796E <sub>H</sub>	CAN Direct Mode Register	CDMR	R/W	CAN clock sync	XXXXXXXX0	
796F <sub>H</sub>	CAN RX/TX redirect register	CANSWR	R/W	CAN 0/1	XXXXXXXX00	

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Address	Register	Abbreviation	Access	Resource name	Initial value
7970 <sub>H</sub>	I <sup>2</sup> C bus status register	IBSR0	R	I <sup>2</sup> C Interface 0	00000000
7971 <sub>H</sub>	I <sup>2</sup> C bus control register	IBCR0	W,R/W		00000000
7972 <sub>H</sub>	I <sup>2</sup> C ten bit slave address register	ITBAL0	R/W		00000000
7973 <sub>H</sub>		ITBAH0	R/W		00000000
7974 <sub>H</sub>	I <sup>2</sup> C ten bit address mask register	ITMKL0	R/W		11111111
7975 <sub>H</sub>		ITMKH0	R/W		00111111
7976 <sub>H</sub>	I <sup>2</sup> C seven bit slave address register	ISBA0	R/W		00000000
7977 <sub>H</sub>	I <sup>2</sup> C seven bit address mask register	ISMK0	R/W		01111111
7978 <sub>H</sub>	I <sup>2</sup> C data register	IDAR0	R/W		00000000
7979 <sub>H</sub> to 797A <sub>H</sub>	Reserved				
797B <sub>H</sub>	I <sup>2</sup> C clock control register	ICCR0	R/W	I <sup>2</sup> C Interface 0	00011111
797C to 797F <sub>H</sub>	Reserved				
7980 <sub>H</sub>	I <sup>2</sup> C bus status register	IBSR1	R	I <sup>2</sup> C Interface 1	00000000
7981 <sub>H</sub>	I <sup>2</sup> C bus control register	IBCR1	W,R/W		00000000
7982 <sub>H</sub>	I <sup>2</sup> C ten bit slave address register	ITBAL1	R/W		00000000
7983 <sub>H</sub>		ITBAH1	R/W		00000000
7984 <sub>H</sub>	I <sup>2</sup> C ten bit address mask register	ITMKL1	R/W		11111111
7985 <sub>H</sub>		ITMKH1	R/W		00111111
7986 <sub>H</sub>	I <sup>2</sup> C seven bit slave address register	ISBA1	R/W		00000000
7987 <sub>H</sub>	I <sup>2</sup> C seven bit address mask register	ISMK1	R/W		01111111
7988 <sub>H</sub>	I <sup>2</sup> C data register	IDAR1	R/W		00000000
7989 <sub>H</sub> to 798A <sub>H</sub>	Reserved				
798B <sub>H</sub>	I <sup>2</sup> C clock control register	ICCR1	R/W	I <sup>2</sup> C Interface 1	00011111
798C <sub>H</sub> to 79C1 <sub>H</sub>	Reserved				
79C2 <sub>H</sub>	Clock Modulator Control Register	CMCR	R,R/W	Clock Modulator	0001X000
79C3 to 79DF <sub>H</sub>	Reserved				

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
79E0 <sub>H</sub>	ROM Correction Address 0	PADR0	R/W	ROM Correction 0	XXXXXXXX
79E1 <sub>H</sub>	ROM Correction Address 0	PADR0	R/W		XXXXXXXX
79E2 <sub>H</sub>	ROM Correction Address 0	PADR0	R/W		XXXXXXXX
79E3 <sub>H</sub>	ROM Correction Address 1	PADR1	R/W		XXXXXXXX
79E4 <sub>H</sub>	ROM Correction Address 1	PADR1	R/W		XXXXXXXX
79E5 <sub>H</sub>	ROM Correction Address 1	PADR1	R/W		XXXXXXXX
79E6 <sub>H</sub>	ROM Correction Address 2	PADR2	R/W		XXXXXXXX
79E7 <sub>H</sub>	ROM Correction Address 2	PADR2	R/W		XXXXXXXX
79E8 <sub>H</sub>	ROM Correction Address 2	PADR2	R/W		XXXXXXXX
79E9 to 79EF <sub>H</sub>	Reserved				
79F0 <sub>H</sub>	ROM Correction Address 3	PADR3	R/W	ROM Correction 1	XXXXXXXX
79F1 <sub>H</sub>	ROM Correction Address 3	PADR3	R/W		XXXXXXXX
79F2 <sub>H</sub>	ROM Correction Address 3	PADR3	R/W		XXXXXXXX
79F3 <sub>H</sub>	ROM Correction Address 4	PADR4	R/W		XXXXXXXX
79F4 <sub>H</sub>	ROM Correction Address 4	PADR4	R/W		XXXXXXXX
79F5 <sub>H</sub>	ROM Correction Address 4	PADR4	R/W		XXXXXXXX
79F6 <sub>H</sub>	ROM Correction Address 5	PADR5	R/W		XXXXXXXX
79F7 <sub>H</sub>	ROM Correction Address 5	PADR5	R/W		XXXXXXXX
79F8 <sub>H</sub>	ROM Correction Address 5	PADR5	R/W		XXXXXXXX
79F9 to 79FF <sub>H</sub>	Reserved				
7A00 to 7AFF <sub>H</sub>	Reserved for CAN Interface 0. Refer to “■ CAN CONTROLLERS”				
7B00 to 7BFF <sub>H</sub>	Reserved for CAN Interface 0. Refer to “■ CAN CONTROLLERS”				
7C00 to 7CFF <sub>H</sub>	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
7D00 to 7DFF <sub>H</sub>	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
7E00 to 7EFF <sub>H</sub>	Reserved for CAN Interface 2. Refer to “■ CAN CONTROLLERS”				
7F00 to 7FFF <sub>H</sub>	Reserved for CAN Interface 2. Refer to “■ CAN CONTROLLERS”				

- Initial value of “X” represents unknown value.
- Addresses in the range 0000<sub>H</sub> to 00BF<sub>H</sub>, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results reading “X” and any write access should not be performed.

## ■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as 1D acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbits/s to 2 Mbits/s (when input clock is at 16 MHz)

**List of Control Registers (1)**

Address			Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2				
000070 <sub>H</sub>	000080 <sub>H</sub>	0000E0 <sub>H</sub>	Message buffer valid register	BVALR	R/W	00000000
000071 <sub>H</sub>	000081 <sub>H</sub>	0000E1 <sub>H</sub>				00000000
000072 <sub>H</sub>	000082 <sub>H</sub>	0000E2 <sub>H</sub>	Transmit request register	TREQR	R/W	00000000
000073 <sub>H</sub>	000083 <sub>H</sub>	0000E3 <sub>H</sub>				00000000
000074 <sub>H</sub>	000084 <sub>H</sub>	0000E4 <sub>H</sub>	Transmit cancel register	TCANR	W	00000000
000075 <sub>H</sub>	000085 <sub>H</sub>	0000E5 <sub>H</sub>				00000000
000076 <sub>H</sub>	000086 <sub>H</sub>	0000E6 <sub>H</sub>	Transmission complete register	TCR	R/W	00000000
000077 <sub>H</sub>	000087 <sub>H</sub>	0000E7 <sub>H</sub>				00000000
000078 <sub>H</sub>	000088 <sub>H</sub>	0000E8 <sub>H</sub>	Receive complete register	RCR	R/W	00000000
000079 <sub>H</sub>	000089 <sub>H</sub>	0000E9 <sub>H</sub>				00000000
00007A <sub>H</sub>	00008A <sub>H</sub>	0000EA <sub>H</sub>	Remote request re- ceiving register	RRTRR	R/W	00000000
00007B <sub>H</sub>	00008B <sub>H</sub>	0000EB <sub>H</sub>				00000000
00007C <sub>H</sub>	00008C <sub>H</sub>	0000EC <sub>H</sub>	Receive overrun register	ROVRR	R/W	00000000
00007D <sub>H</sub>	00008D <sub>H</sub>	0000ED <sub>H</sub>				00000000
00007E <sub>H</sub>	00008E <sub>H</sub>	0000EE <sub>H</sub>	Reception interrupt enable register	RIER	R/W	00000000
00007F <sub>H</sub>	00008F <sub>H</sub>	0000EF <sub>H</sub>				00000000

List of Control Registers (2)

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
007B00H	007D00H	007F00H	Control status register	CSR	R/W, W R/W, R	0XXXX0X1
007B01H	007D01H	007F01H				00XXX000
007B02H	007D02H	007F02H	Last event indicator register	LEIR	R/W	000X0000
007B03H	007D03H	007F03H				XXXXXXXX
007B04H	007D04H	007F04H	Receive/transmit error counter	RTEC	R	00000000
007B05H	007D05H	007F05H				00000000
007B06H	007D06H	007F06H	Bit timing register	BTR	R/W	11111111
007B07H	007D07H	007F07H				X1111111
007B08H	007D08H	007F08H	IDE register	IDER	R/W	XXXXXXXX
007B09H	007D09H	007F09H				XXXXXXXX
007B0AH	007D0AH	007F0AH	Transmit RTR register	TRTRR	R/W	00000000
007B0BH	007D0BH	007F0BH				00000000
007B0CH	007D0CH	007F0CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX
007B0DH	007D0DH	007F0DH				XXXXXXXX
007B0EH	007D0EH	007F0EH	Transmit interrupt enable register	TIER	R/W	00000000
007B0FH	007D0FH	007F0FH				00000000
007B10H	007D10H	007F10H	Acceptance mask select register	AMSR	R/W	XXXXXXXX
007B11H	007D11H	007F11H				XXXXXXXX
007B12H	007D12H	007F12H				XXXXXXXX
007B13H	007D13H	007F13H				XXXXXXXX
007B14H	007D14H	007F14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX
007B15H	007D15H	007F15H				XXXXXXXX
007B16H	007D16H	007F16H				XXXXXXXX
007B17H	007D17H	007F17H				XXXXXXXX
007B18H	007D18H	007F18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX
007B19H	007D19H	007F19H				XXXXXXXX
007B1AH	007D1AH	007F1AH				XXXXXXXX
007B1BH	007D1BH	007F1BH				XXXXXXXX

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List of Message Buffers (ID Registers) (1)

Address			Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2				
007A00H to 007A1FH	007C00H to 007C1FH	007E00H to 007E1FH	General- purpose RAM	—	R/W	XXXXXXXX to XXXXXXXX
007A20H	007C20H	007E20H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXX
007A21H	007C21H	007E21H				
007A22H	007C22H	007E22H				
007A23H	007C23H	007E23H				
007A24H	007C24H	007E24H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXX
007A25H	007C25H	007E25H				
007A26H	007C26H	007E26H				
007A27H	007C27H	007E27H				
007A28H	007C28H	007E28H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXX
007A29H	007C29H	007E29H				
007A2AH	007C2AH	007E2AH				
007A2BH	007C2BH	007E2BH				
007A2CH	007C2CH	007E2CH	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX
007A2DH	007C2DH	007E2DH				
007A2EH	007C2EH	007E2EH				
007A2FH	007C2FH	007E2FH				
007A30H	007C30H	007E30H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX
007A31H	007C31H	007E31H				
007A32H	007C32H	007E32H				
007A33H	007C33H	007E33H				
007A34H	007C34H	007E34H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX
007A35H	007C35H	007E35H				
007A36H	007C36H	007E36H				
007A37H	007C37H	007E37H				
007A38H	007C38H	007E38H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX
007A39H	007C39H	007E39H				
007A3AH	007C3AH	007E3AH				
007A3BH	007C3BH	007E3BH				
007A3CH	007C3CH	007E3CH	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX
007A3DH	007C3DH	007E3DH				
007A3EH	007C3EH	007E3EH				
007A3FH	007C3FH	007E3FH				

List of Message Buffers (ID Registers) (2)

Address			Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2				
007A40H	007C40H	007E40H	ID register 8	IDR8	R/W	XXXXXXXX
007A41H	007C41H	007E41H				XXXXXXXX
007A42H	007C42H	007E42H				XXXXXXXX
007A43H	007C43H	007E43H				XXXXXXXX
007A44H	007C44H	007E44H	ID register 9	IDR9	R/W	XXXXXXXX
007A45H	007C45H	007E45H				XXXXXXXX
007A46H	007C46H	007E46H				XXXXXXXX
007A47H	007C47H	007E47H				XXXXXXXX
007A48H	007C48H	007E48H	ID register 10	IDR10	R/W	XXXXXXXX
007A49H	007C49H	007E49H				XXXXXXXX
007A4AH	007C4AH	007E4AH				XXXXXXXX
007A4BH	007C4BH	007E4BH				XXXXXXXX
007A4CH	007C4CH	007E4CH	ID register 11	IDR11	R/W	XXXXXXXX
007A4DH	007C4DH	007E4DH				XXXXXXXX
007A4EH	007C4EH	007E4EH				XXXXXXXX
007A4FH	007C4FH	007E4FH				XXXXXXXX
007A50H	007C50H	007E50H	ID register 12	IDR12	R/W	XXXXXXXX
007A51H	007C51H	007E51H				XXXXXXXX
007A52H	007C52H	007E52H				XXXXXXXX
007A53H	007C53H	007E53H				XXXXXXXX
007A54H	007C54H	007E54H	ID register 13	IDR13	R/W	XXXXXXXX
007A55H	007C55H	007E55H				XXXXXXXX
007A56H	007C56H	007E56H				XXXXXXXX
007A57H	007C57H	007E57H				XXXXXXXX
007A58H	007C58H	007E58H	ID register 14	IDR14	R/W	XXXXXXXX
007A59H	007C59H	007E59H				XXXXXXXX
007A5AH	007C5AH	007E5AH				XXXXXXXX
007A5BH	007C5BH	007E5BH				XXXXXXXX
007A5CH	007C5CH	007E5CH	ID register 15	IDR15	R/W	XXXXXXXX
007A5DH	007C5DH	007E5DH				XXXXXXXX
007A5EH	007C5EH	007E5EH				XXXXXXXX
007A5FH	007C5FH	007E5FH				XXXXXXXX

# MB90340 Series

List of Message Buffers (DLC Registers and Data Registers) (1)

Address			Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2				
007A60H	007C60H	007E60H	DLC register 0	DLCR0	R/W	XXXXXXXX
007A61H	007C61H	007E61H				
007A62H	007C62H	007E62H	DLC register 1	DLCR1	R/W	XXXXXXXX
007A63H	007C63H	007E63H				
007A64H	007C64H	007E64H	DLC register 2	DLCR2	R/W	XXXXXXXX
007A65H	007C65H	007E65H				
007A66H	007C66H	007E66H	DLC register 3	DLCR3	R/W	XXXXXXXX
007A67H	007C67H	007E67H				
007A68H	007C68H	007E68H	DLC register 4	DLCR4	R/W	XXXXXXXX
007A69H	007C69H	007E69H				
007A6AH	007C6AH	007E6AH	DLC register 5	DLCR5	R/W	XXXXXXXX
007A6BH	007C6BH	007E6BH				
007A6CH	007C6CH	007E6CH	DLC register 6	DLCR6	R/W	XXXXXXXX
007A6DH	007C6DH	007E6DH				
007A6EH	007C6EH	007E6EH	DLC register 7	DLCR7	R/W	XXXXXXXX
007A6FH	007C6FH	007E6FH				
007A70H	007C70H	007E70H	DLC register 8	DLCR8	R/W	XXXXXXXX
007A71H	007C71H	007E71H				
007A72H	007C72H	007E72H	DLC register 9	DLCR9	R/W	XXXXXXXX
007A73H	007C73H	007E73H				
007A74H	007C74H	007E74H	DLC register 10	DLCR10	R/W	XXXXXXXX
007A75H	007C75H	007E75H				
007A76H	007C76H	007E76H	DLC register 11	DLCR11	R/W	XXXXXXXX
007A77H	007C77H	007E77H				
007A78H	007C78H	007E78H	DLC register 12	DLCR12	R/W	XXXXXXXX
007A79H	007C79H	007E79H				
007A7AH	007C7AH	007E7AH	DLC register 13	DLCR13	R/W	XXXXXXXX
007A7BH	007C7BH	007E7BH				
007A7CH	007C7CH	007E7CH	DLC register 14	DLCR14	R/W	XXXXXXXX
007A7DH	007C7DH	007E7DH				
007A7EH	007C7EH	007E7EH	DLC register 15	DLCR15	R/W	XXXXXXXX
007A7FH	007C7FH	007E7FH				

List of Message Buffers (DLC Registers and Data Registers) (2)

Address			Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2				
007A80H to 007A87H	007C80H to 007C87H	007E80H to 007E87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX to XXXXXXXX
007A88H to 007A8FH	007C88H to 007C8FH	007E88H to 007E8FH	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX to XXXXXXXX
007A90H to 007A97H	007C90H to 007C97H	007E90H to 007E97H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX to XXXXXXXX
007A98H to 007A9FH	007C98H to 007C9FH	007E98H to 007E9FH	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX to XXXXXXXX
007AA0H to 007AA7H	007CA0H to 007CA7H	007EA0H to 007EA7H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX to XXXXXXXX
007AA8H to 007AAFH	007CA8H to 007CAFH	007EA8H to 007EAFH	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX to XXXXXXXX
007AB0H to 007AB7H	007CB0H to 007CB7H	007EB0H to 007EB7H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX to XXXXXXXX
007AB8H to 007ABFH	007CB8H to 007CBFH	007EB8H to 007EBFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX to XXXXXXXX
007AC0H to 007AC7H	007CC0H to 007CC7H	007EC0H to 007EC7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX to XXXXXXXX
007AC8H to 007ACFH	007CC8H to 007CCFH	007EC8H to 007ECFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX to XXXXXXXX
007AD0H to 007AD7H	007CD0H to 007CD7H	007ED0H to 007ED7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX to XXXXXXXX
007AD8H to 007ADFH	007CD8H to 007CDFH	007ED8H to 007EDFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX to XXXXXXXX
007AE0H to 007AE7H	007CE0H to 007CE7H	007EE0H to 007EE7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX to XXXXXXXX
007AE8H to 007AEFH	007CE8H to 007CEFH	007EE8H to 007EEFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX to XXXXXXXX

# MB90340 Series

List of Message Buffers (DLC Registers and Data Registers) (3)

Address			Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2				
007AF0 <sub>H</sub> to 007AF7 <sub>H</sub>	007CF0 <sub>H</sub> to 007CF7 <sub>H</sub>	007EF0 <sub>H</sub> to 007EF7 <sub>H</sub>	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX to XXXXXXXX
007AF8 <sub>H</sub> to 007AFF <sub>H</sub>	007CF8 <sub>H</sub> to 007CFF <sub>H</sub>	007EF8 <sub>H</sub> to 007EFF <sub>H</sub>	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX to XXXXXXXX

PRELIMINARY

## ■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI <sup>2</sup> OS clear	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC <sub>H</sub>	—	—
INT9 instruction	N	—	#09	FFFFD8 <sub>H</sub>	—	—
Exception	N	—	#10	FFFFD4 <sub>H</sub>	—	—
CAN 0 RX	N	—	#11	FFFFD0 <sub>H</sub>	ICR00	0000B0 <sub>H</sub>
CAN 0 TX/NS	Y1	—	#12	FFFFCC <sub>H</sub>		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8 <sub>H</sub>	ICR01	0000B1 <sub>H</sub>
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4 <sub>H</sub>		
CAN 2 RX / I2C0	N	—	#15	FFFFC0 <sub>H</sub>	ICR02	0000B2 <sub>H</sub>
CAN 2 TX/NS	N	—	#16	FFFFBC <sub>H</sub>		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8 <sub>H</sub>	ICR03	0000B3 <sub>H</sub>
16-bit Reload Timer 1	Y1	1	#18	FFFFB4 <sub>H</sub>		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0 <sub>H</sub>	ICR04	0000B4 <sub>H</sub>
16-bit Reload Timer 3	Y1	—	#20	FFFFAC <sub>H</sub>		
PPG 0/1/4/5	N	—	#21	FFFFA8 <sub>H</sub>	ICR05	0000B5 <sub>H</sub>
PPG 2/3/6/7	N	—	#22	FFFFA4 <sub>H</sub>		
PPG 8/9/C/D	N	—	#23	FFFFA0 <sub>H</sub>	ICR06	0000B6 <sub>H</sub>
PPG A/B/E/F	N	—	#24	FFFF9C <sub>H</sub>		
Time Base Timer	N	—	#25	FFFF98 <sub>H</sub>	ICR07	0000B7 <sub>H</sub>
External Interrupt 0-3, 8-11	Y1	3	#26	FFFF94 <sub>H</sub>		
Watch Timer	N	—	#27	FFFF90 <sub>H</sub>	ICR08	0000B8 <sub>H</sub>
External Interrupt 4-7, 12-15	Y1	4	#28	FFFF8C <sub>H</sub>		
A/D Converter	Y1	5	#29	FFFF88 <sub>H</sub>	ICR09	0000B9 <sub>H</sub>
I/O Timer 0 / I/O Timer 1	N	—	#30	FFFF84 <sub>H</sub>		
Input Capture 4/5 / I2C1	Y1	6	#31	FFFF80 <sub>H</sub>	ICR10	0000BA <sub>H</sub>
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C <sub>H</sub>		
Input Capture 0-3	Y1	8	#33	FFFF78 <sub>H</sub>	ICR11	0000BB <sub>H</sub>
Output Compare 2/3/6/7	Y1	9	#34	FFFF74 <sub>H</sub>		
UART 0 RX	Y2	10	#35	FFFF70 <sub>H</sub>	ICR12	0000BC <sub>H</sub>
UART 0 TX	Y1	11	#36	FFFF6C <sub>H</sub>		
UART 1 RX / UART 3 RX	Y2	12	#37	FFFF68 <sub>H</sub>	ICR13	0000BD <sub>H</sub>
UART 1 TX / UART 3 TX	Y1	13	#38	FFFF64 <sub>H</sub>		

(Continued)

(Continued)

Interrupt cause	EI <sup>2</sup> OS clear	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 RX / UART 4 RX	Y2	14	#39	FFFF60 <sub>H</sub>	ICR14	0000BE <sub>H</sub>
UART 2 TX / UART 4 TX	Y1	15	#40	FFFF5C <sub>H</sub>		
Flash Memory	N	—	#41	FFFF58 <sub>H</sub>	ICR15	0000BF <sub>H</sub>
Delayed interrupt	N	—	#42	FFFF54 <sub>H</sub>		

Y1 : The interrupt request flag is cleared by the EI<sup>2</sup>OS interrupt clear signal.a

Y2 : The interrupt request flag is cleared by the EI<sup>2</sup>OS interrupt clear signal. A stop request is available.

N : The interrupt request flag is not cleared by the EI<sup>2</sup>OS interrupt clear signal.

Notes : For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI<sup>2</sup>OS interrupt clear signal.

At the end of EI<sup>2</sup>OS, the EI<sup>2</sup>OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI<sup>2</sup>OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI<sup>2</sup>OS clear signal caused by the first event. So it is recommended not to use the EI<sup>2</sup>OS for this interrupt number.

If EI<sup>2</sup>OS is enabled, EI<sup>2</sup>OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI<sup>2</sup>OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI<sup>2</sup>OS, the other interrupt should be disabled.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

( $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	$AV_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC} * 1$
	$AV_{RH}, AV_{RL}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AV_{RH}, AV_{CC} \geq AV_{RL}, AV_{RH} \geq AV_{RL}$
Input voltage	$V_I$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Output voltage	$V_O$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Maximum Clamp Current	$I_{CLAMP}$	-2.0	+2.0	mA	*4
Total Maximum Clamp Current	$\Sigma I_{CLAMP} $	—	20	mA	*4
“L” level maximum output current	$I_{OL1}$	—	15	mA	*3
“L” level average output current	$I_{OLAV1}$	—	4	mA	*3
“L” level maximum overall output current	$\Sigma I_{OL1}$	—	100	mA	*3
“L” level average overall output current	$\Sigma I_{OLAV1}$	—	50	mA	*3
“H” level maximum output current	$I_{OH1}$	—	-15	mA	*3
“H” level average output current	$I_{OHAV1}$	—	-4	mA	*3
“H” level maximum overall output current	$\Sigma I_{OH1}$	—	-100	mA	*3
“H” level average overall output current	$\Sigma I_{OHAV1}$	—	-50	mA	*3
Power consumption	$P_D$	—	500	mW	MB90F347
Operating temperature	$T_A$	-40	+105	°C	
Storage temperature	$T_{STG}$	-55	+150	°C	

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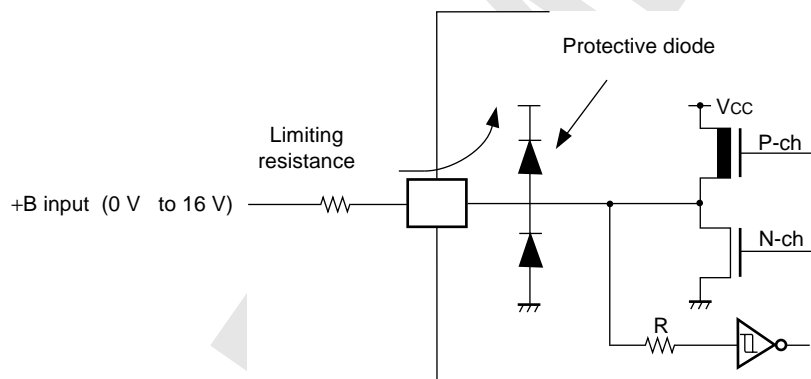
PRELIMINARY

# MB90340 Series

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- \*1: Set  $AV_{CC}$  and  $V_{CC}$  to the same voltage. Make sure that  $AV_{CC}$  does not exceed  $V_{CC}$  and that the voltage at the analog inputs does not exceed  $AV_{CC}$  when the power is switched on.
- \*2:  $V_I$  and  $V_O$  should not exceed  $V_{CC} + 0.3$  V.  $V_I$  should not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the  $I_{CLAMP}$  rating supercedes the  $V_I$  rating.
- \*3: Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1
- \*5:
  - Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1
  - Use within recommended operating conditions.
  - Use at DC voltage (current)
  - The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
  - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
  - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the  $V_{CC}$  pin, and this may affect other devices.
  - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
  - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
  - Care must be taken not to leave the +B input pin open.
  - Sample recommended circuits:

- Input/output equivalent circuits



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Conditions

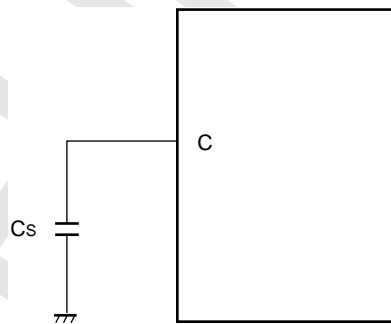
( $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{CC}$ $AV_{CC}$	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter
		4.5	5.0	5.5	V	When writing to Flash memory
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smooth capacitor	$C_S$	0.1	0.33	1.0	$\mu\text{F}$	Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the $V_{CC}$ should be greater than this capacitor.
Operating temperature	$T_A$	-40	—	+105	$^{\circ}\text{C}$	

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.



**C Pin Connection Diagram**

# MB90340 Series

## 3. DC Characteristics

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At $V_{CC} = 5\text{ V} \pm 10\%$ )	$V_{IHS}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if CMOS hysteresis input levels are selected (except I <sup>2</sup> C input pins)
	$V_{IHA}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if AUTOMOTIVE input levels are selected
	$V_{IHT}$	—	—	2.0	—	$V_{CC} + 0.3$	V	Port inputs if TTL input levels are selected
	$V_{IHI}$	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	I <sup>2</sup> C Port inputs if CMOS hysteresis input levels are selected
	$V_{IHR}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{RST}$ input pin (CMOS hysteresis)
	$V_{IHM}$	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input L voltage (At $V_{CC} = 5\text{ V} \pm 10\%$ )	$V_{ILS}$	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Port inputs if CMOS hysteresis input levels are selected (except I <sup>2</sup> C input pins)
	$V_{ILA}$	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Port inputs if AUTOMOTIVE input levels are selected
	$V_{ILT}$	—	—	$V_{SS} - 0.3$	—	0.8	V	Port inputs if TTL input levels are selected
	$V_{ILI}$	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	I <sup>2</sup> C Port inputs if CMOS hysteresis input levels are selected
	$V_{ILR}$	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	$\overline{RST}$ input pin (CMOS hysteresis)
	$V_{ILM}$	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output H voltage	$V_{OH1}$	Normal outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OH1} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output H voltage	$V_{OH2}$	I <sup>2</sup> C current outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OH2} = -3.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	$V_{OL1}$	Normal outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OL1} = 4.0\text{ mA}$	—	—	0.4	V	
Output L voltage	$V_{OL2}$	I <sup>2</sup> C current outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OL2} = 3.0\text{ mA}$	—	—	0.4	V	
Input leak current	$I_{IL}$	—	$V_{CC} = 5.5\text{ V}$ , $V_{SS} < V_I < V_{CC}$	-5	—	5	$\mu\text{A}$	

(Continued)

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub> = 5.0 V, Internal frequency : 24 MHz, At normal operation.	—	60	80	mA	MB90F347
			V <sub>CC</sub> = 5.0 V, Internal frequency : 24 MHz, At writing FLASH memory.	—	75	95	mA	MB90F347
			V <sub>CC</sub> = 5.0 V, Internal frequency : 24 MHz, At erasing FLASH memory.	—	80	100	mA	MB90F347
	I <sub>CCS</sub>		V <sub>CC</sub> = 5.0 V, Internal frequency : 24 MHz, At Sleep mode.	—	25	35	mA	MB90F347
	I <sub>CTS</sub>		V <sub>CC</sub> = 5.0 V, Internal frequency : 2 MHz, At Main Timer mode	—	0.6	TBD	mA	MB90F347
	I <sub>CTSPLL4</sub>		V <sub>CC</sub> = 5.0 V, Internal frequency : 24 MHz, At PLL Timer mode, external frequency = 4 MHz	—	5	7	mA	MB90F347
	I <sub>CCL</sub>		V <sub>CC</sub> = 5.0V Internal frequency: 8 kHz, At sub operation T <sub>A</sub> = 25°C	—	TBD	TBD	μA	MB90F347
	I <sub>CCLS</sub>		V <sub>CC</sub> = 5.0V Internal frequency: 8 kHz, At sub sleep T <sub>A</sub> = 25°C	—	TBD	TBD	μA	MB90F347
	I <sub>CCW</sub>		V <sub>CC</sub> = 5.0V Internal frequency: 8 kHz, At watch mode T <sub>A</sub> = 25°C	—	TBD	TBD	μA	MB90F347
	I <sub>CCH</sub>		V <sub>CC</sub> = 5.0 V, At Stop mode, T <sub>A</sub> = +25°C	—	5	TBD	μA	MB90F347
Input capacity	C <sub>IN</sub>	Other than C, AV <sub>CC</sub> , AV <sub>SS</sub> , AVRH, AVRL, V <sub>CC</sub> , V <sub>SS</sub> , DV <sub>CC</sub> , DV <sub>SS</sub> ,	—	—	5	15	pF	

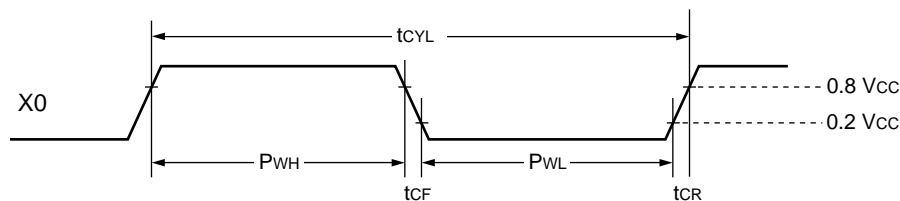
\* : Current values are tentative. They are subject to change without notice according to improvements in the characteristics. The power supply current is measured with an external clock.

## 4. AC Characteristics

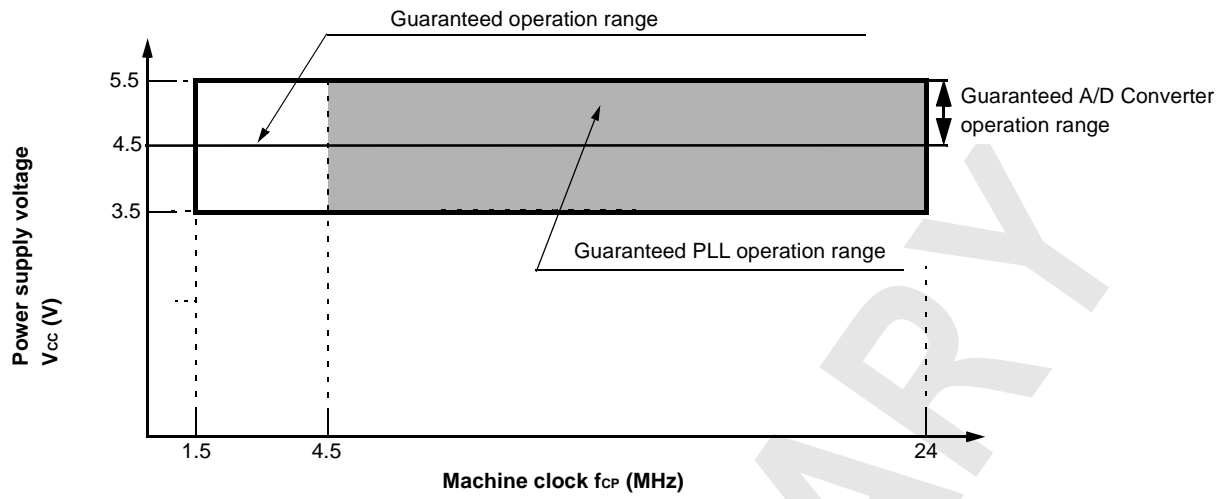
### (1) Clock Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

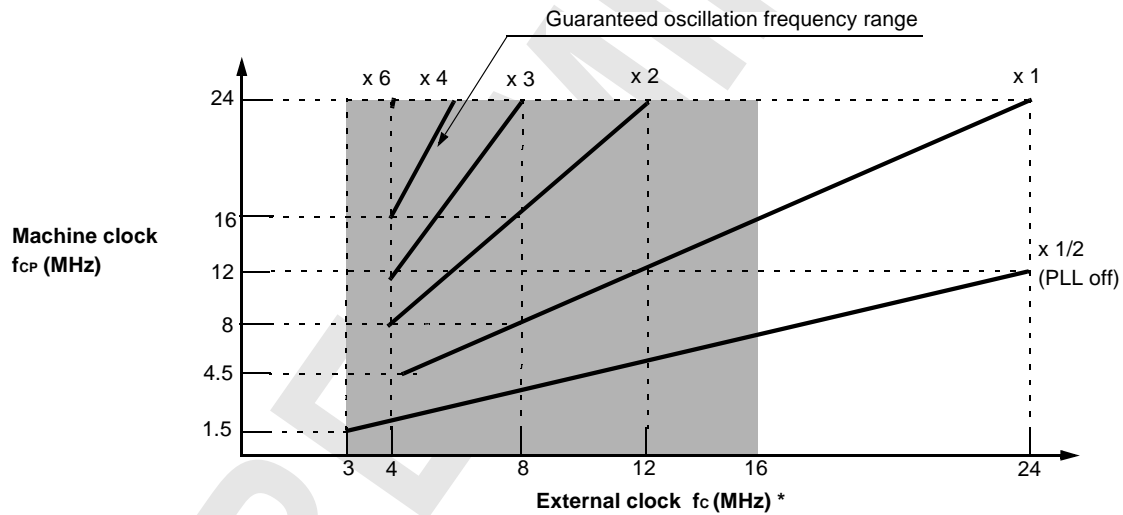
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Oscillation frequency	$f_c$	X0, X1	3	—	16	MHz	When using an oscillation circuit
		X0, X1	3	—	24	MHz	When using an external clock
	$t_{cL}$	X0A, X1A	—	32.768	100	kHz	
Oscillation cycle time	$t_{cYL}$	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	$t_{cYLL}$	X0A, X1A	10	30.5	—	$\mu\text{s}$	
Input clock pulse width	$P_{WH}, P_{WL}$	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	$P_{WHL}, P_{WLL}$	X0A	5	15.2	—	$\mu\text{s}$	
Input clock rise and fall time	$t_{cR}, t_{cF}$	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	$f_{cP}$	—	1.5	—	24	MHz	When using main clock
	$f_{cPL}$	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	$t_{cP}$	—	41.67	—	666	ns	When using main clock
	$t_{cPL}$	—	20	122.1	—	$\mu\text{s}$	When using sub clock



**Clock Timing**



## Guaranteed operation range of MB90F347



\* : When using the oscillation circuit, the maximum oscillation clock frequency is 16 MHz

## External clock frequency and Machine clock frequency

## (2) Reset Standby Input

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ )

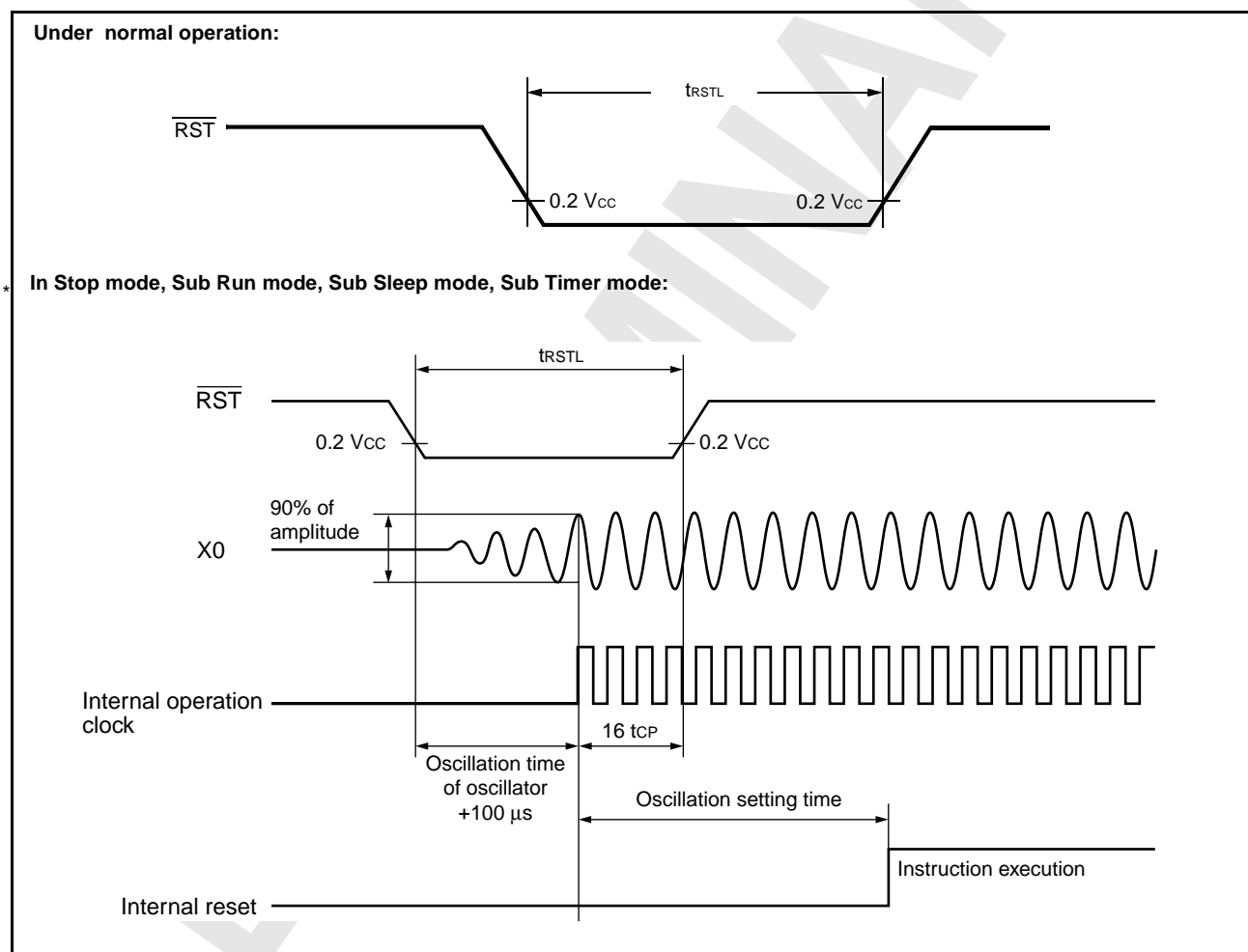
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	$t_{RSTL}$	$\overline{RST}$	$16\ t_{CP}^{*1}$	—	ns	Under normal operation
			Oscillation time of oscillator <sup>*2</sup> + $100\ \mu\text{s} + 16\ t_{CP}^{*1}$	—	ns	In Stop mode, Sub Run mode, Sub Sleep mode and Sub Timer mode
			100	—	$\mu\text{s}$	In Main Timer mode

\*1 : “ $t_{CP}$ ” represents one cycle time of the machine clock.

No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

\*2 : Oscillation time of oscillator is the time that the amplitude reaches 90%.

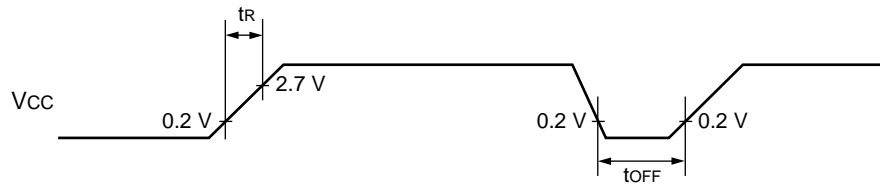
In the crystal oscillator, the oscillation time is between several ms and to tens of ms. In FAR / ceramic oscillators, the oscillation time is between hundreds of  $\mu\text{s}$  to several ms. With an external clock, the oscillation time is 0 ms.



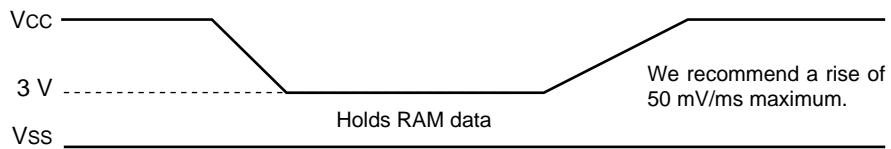
## (3) Power On Reset

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	$t_R$	$V_{CC}$	—	0.05	30	ms	
Power off time	$t_{OFF}$	$V_{CC}$		50	—	ms	Due to repetitive operation



If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



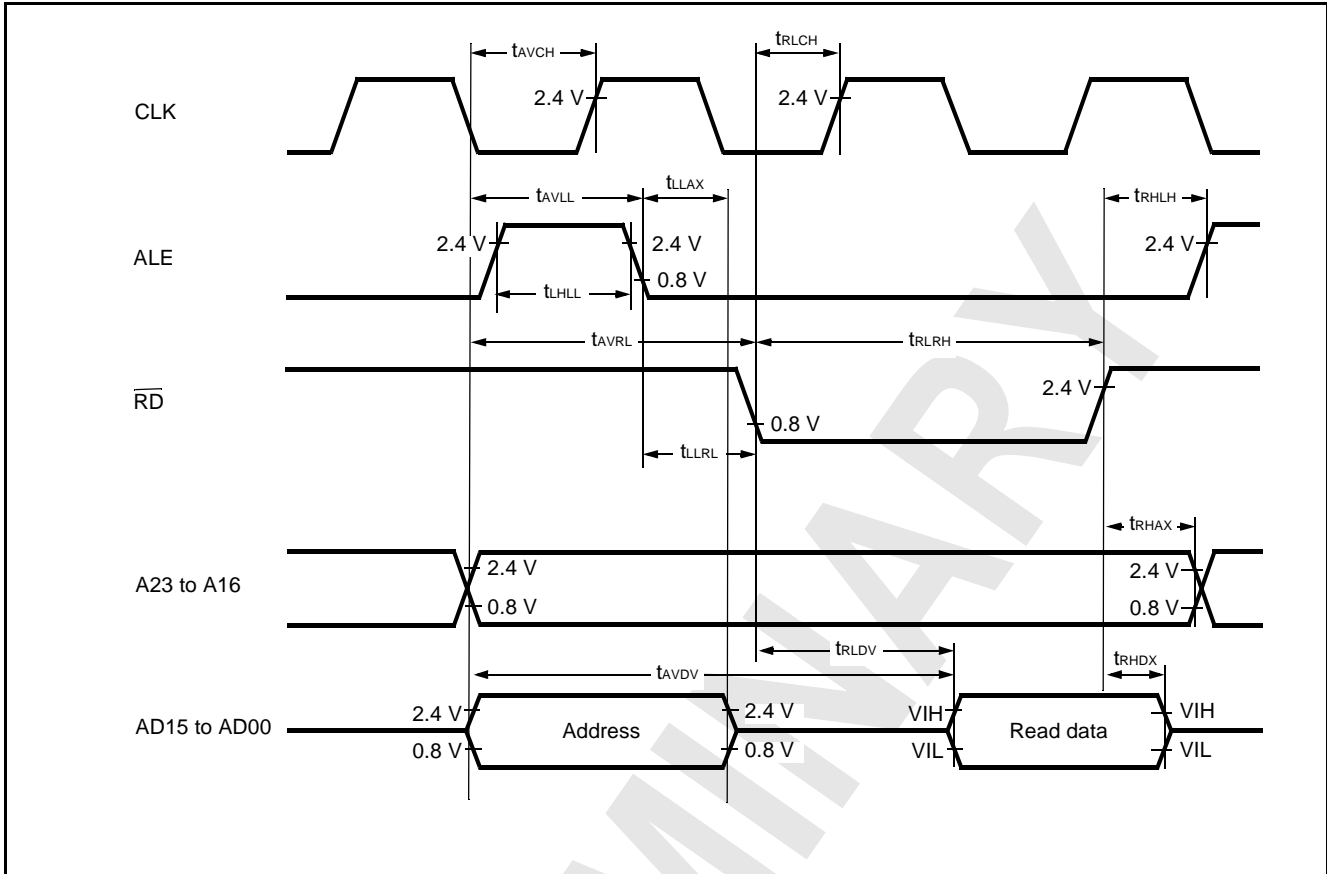
PRELIMINARY

# MB90340 Series

## (4) Bus Timing (Read)

( $T_A = -40^\circ$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 4.5$  to  $5.5\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min.	Max.		
ALE pulse width	$t_{LHLL}$	ALE	—	$t_{CP}/2 - 10$	—	ns	
Valid address $\Rightarrow$ ALE $\downarrow$ time	$t_{AVLL}$	ALE, A23 to A16, AD15 to AD00	—	$t_{CP}/2 - 15$	—	ns	
ALE $\downarrow \Rightarrow$ Address valid time	$t_{LLAX}$	ALE, AD15 to AD00	—	$t_{CP}/2 - 15$	—	ns	
Valid address $\Rightarrow \overline{RD} \downarrow$ time	$t_{AVRL}$	A23 to A16, AD15 to AD00, $\overline{RD}$	—	$t_{CP} - 15$	—	ns	
Valid address $\Rightarrow$ Valid data input	$t_{AVDV}$	A23 to A16, AD15 to AD00	—	—	$5 t_{CP}/2 - 40$	ns	
$\overline{RD}$ pulse width	$t_{RLRH}$	$\overline{RD}$	—	$3 t_{CP}/2 - 20$	—	ns	
$\overline{RD} \downarrow \Rightarrow$ Valid data input	$t_{RLDV}$	$\overline{RD}$ , AD15 to AD00	—	—	$3 t_{CP}/2 - 50$	ns	
$\overline{RD} \uparrow \Rightarrow$ Data hold time	$t_{RHDX}$	$\overline{RD}$ , AD15 to AD00	—	0	—	ns	
$\overline{RD} \downarrow \Rightarrow$ ALE $\uparrow$ time	$t_{RHLH}$	$\overline{RD}$ , ALE	—	$t_{CP}/2 - 15$	—	ns	
$\overline{RD} \uparrow \Rightarrow$ Address valid time	$t_{RHAX}$	$\overline{RD}$ , A23 to A16	—	$t_{CP}/2 - 10$	—	ns	
Valid address $\Rightarrow$ CLK $\uparrow$ time	$t_{AVCH}$	A23 to A16, AD15 to AD00, CLK	—	$t_{CP}/2 - 15$	—	ns	
$\overline{RD} \downarrow \Rightarrow$ CLK $\uparrow$ time	$t_{RLCH}$	$\overline{RD}$ , CLK	—	$t_{CP}/2 - 15$	—	ns	
ALE $\downarrow \Rightarrow \overline{RD} \downarrow$ time	$t_{LLRL}$	ALE, $\overline{RD}$	—	$t_{CP}/2 - 15$	—	ns	



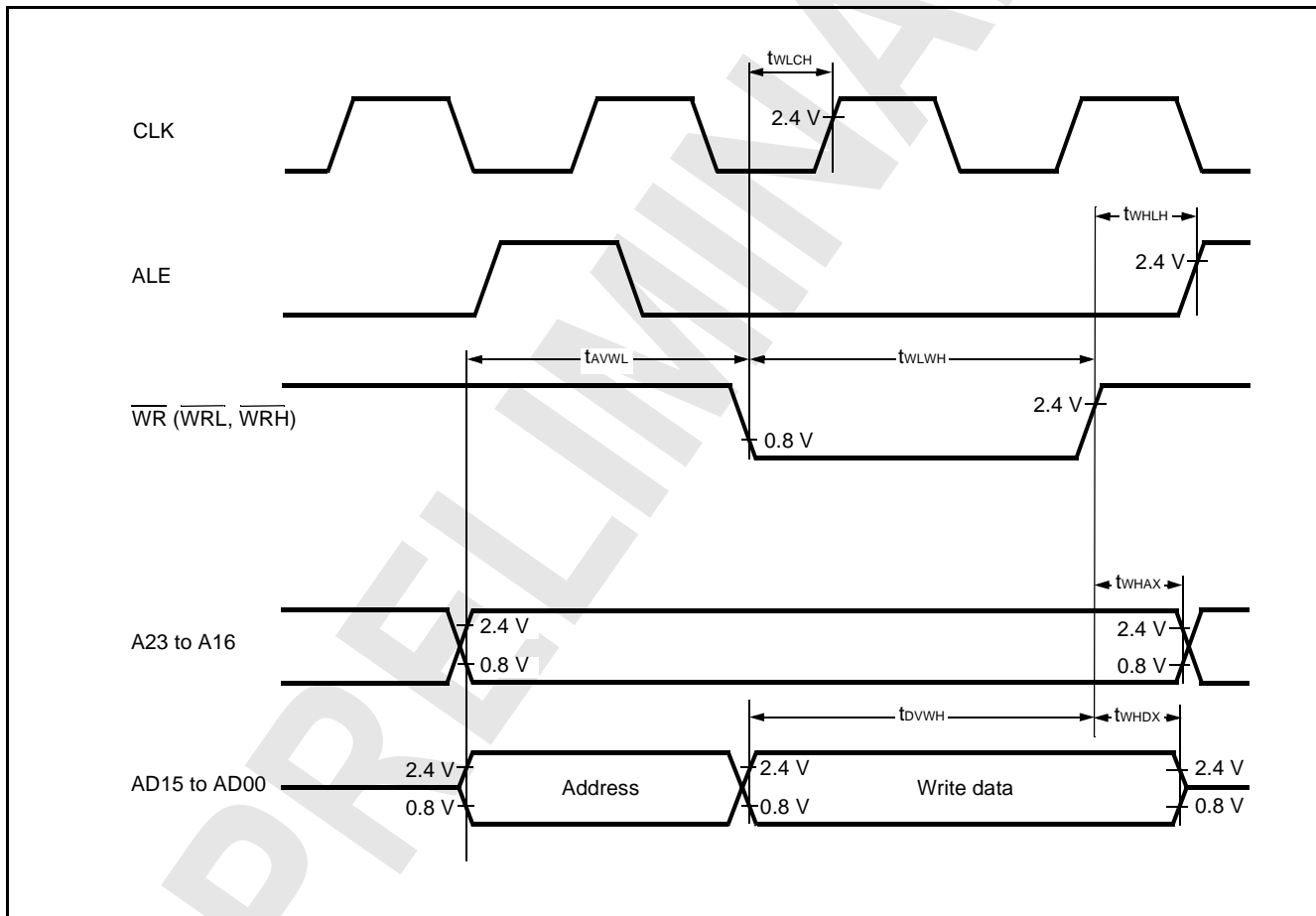
PRELIMINARY

# MB90340 Series

## (5) Bus Timing (Write)

( $T_A = -40^\circ$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 4.5$  to  $5.5\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min.	Max.		
Valid address $\Rightarrow \overline{\text{WR}} \downarrow$ time	$t_{\text{AVWL}}$	A23 to A16, AD15 to AD00, $\overline{\text{WR}}$	—	$t_{\text{CP}} - 15$	—	ns	
$\overline{\text{WR}}$ pulse width	$t_{\text{WLWH}}$	$\overline{\text{WR}}$		$3 t_{\text{CP}}/2 - 20$	—	ns	
Valid data output $\Rightarrow \overline{\text{WR}} \uparrow$ time	$t_{\text{DVWH}}$	AD15 to AD00, $\overline{\text{WR}}$		$3 t_{\text{CP}}/2 - 20$	—	ns	
$\overline{\text{WR}} \uparrow \Rightarrow$ Data hold time	$t_{\text{WHDX}}$	AD15 to AD00, $\overline{\text{WR}}$		<b>15</b>	—	ns	
$\overline{\text{WR}} \uparrow \Rightarrow$ Address valid time	$t_{\text{WHAX}}$	A23 to A16, $\overline{\text{WR}}$		$t_{\text{CP}}/2 - 10$	—	ns	
$\overline{\text{WR}} \uparrow \Rightarrow$ ALE $\uparrow$ time	$t_{\text{WHLH}}$	$\overline{\text{WR}}$ , ALE		$t_{\text{CP}}/2 - 15$	—	ns	
$\overline{\text{WR}} \downarrow \Rightarrow$ CLK $\uparrow$ time	$t_{\text{WLCH}}$	$\overline{\text{WR}}$ , CLK		$t_{\text{CP}}/2 - 15$	—	ns	

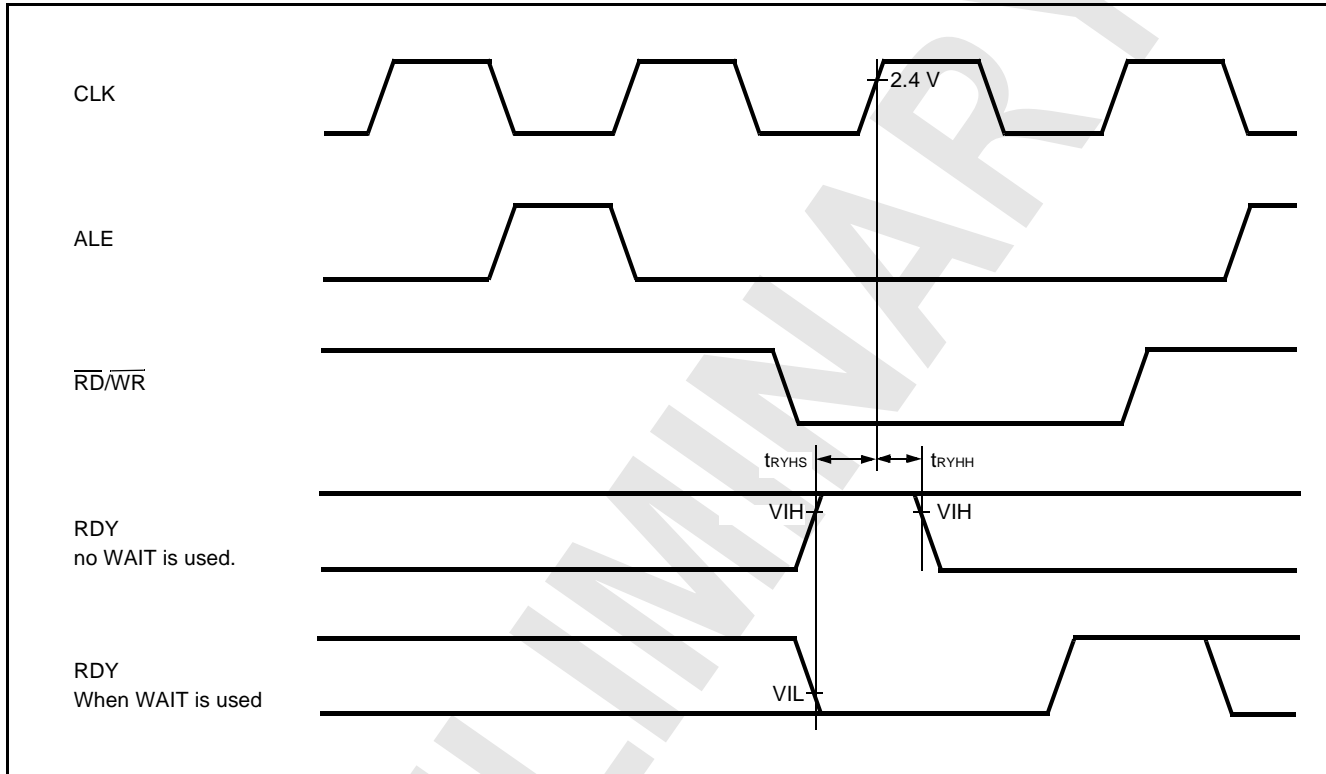


## (6) Ready Input Timing

( $T_A = -40^\circ$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 4.5$  to  $5.5\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min.	Max.		
RDY setup time	$t_{RYHS}$	RDY	—	45	—	ns	
RDY hold time	$t_{RYHH}$	RDY		0	—	ns	

Note: If the RDY setup time is insufficient, use the auto-ready function.



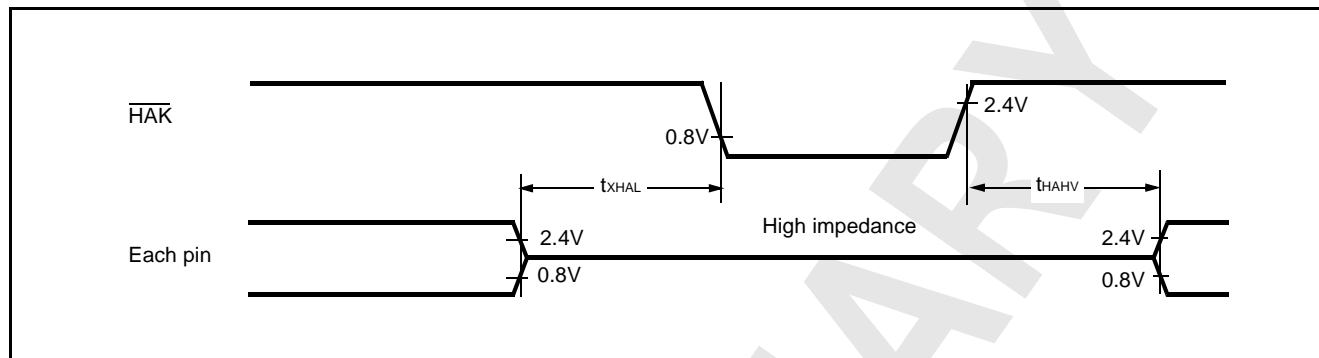
# MB90340 Series

## (7) Hold Timing

( $T_A = -40^\circ$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 4.5$  to  $5.5$  V,  $V_{SS} = 0.0$  V)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min.	Max.		
Pin floating $\Rightarrow$ $\overline{\text{HAK}} \downarrow$ time	$t_{\text{XHAL}}$	$\overline{\text{HAK}}$	—	30	$t_{\text{CP}}$	ns	
$\overline{\text{HAK}} \uparrow$ time $\Rightarrow$ Pin valid time	$t_{\text{HAHV}}$	$\overline{\text{HAK}}$		$t_{\text{CP}}$	$2 t_{\text{CP}}$	ns	

Note: There is more than 1 cycle from when HRQ reads in until the  $\overline{\text{HAK}}$  is changed.

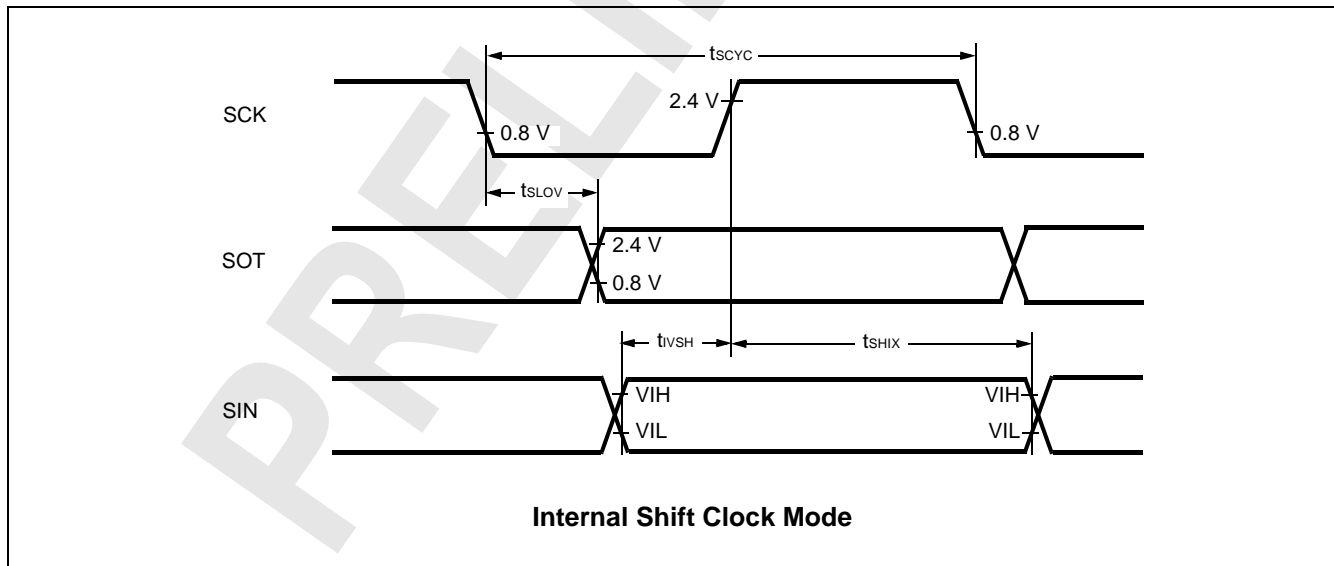


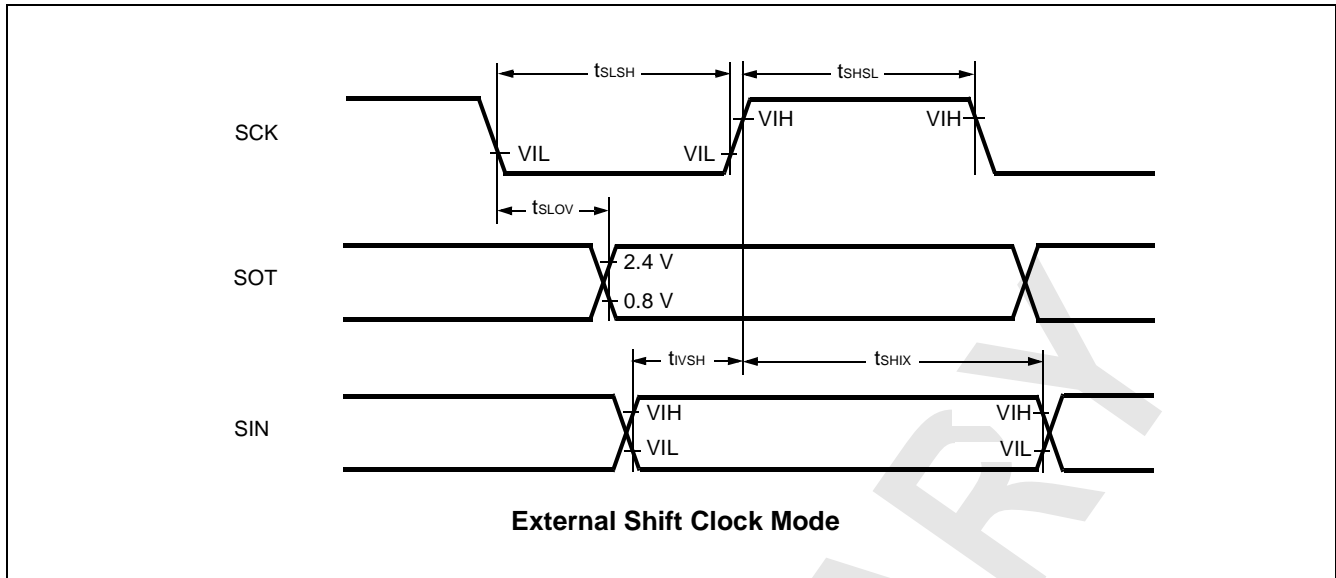
## (8) UART0/1/2/3/4

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	SCK0 to SCK4	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$8 t_{CP}$	—	ns	
SCK ↓ → SOT delay time	$t_{SLOV}$	SCK0 to SCK4, SOT0 to SOT4		-80	+80	ns	
Valid SIN → SCK ↑	$t_{VSH}$	SCK0 to SCK4, SIN0 to SIN4		100	—	ns	
SCK ↑ → Valid SIN hold time	$t_{SHIX}$	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	
Serial clock "H" pulse width	$t_{SHSL}$	SCK0 to SCK4	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$4 t_{CP}$	—	ns	
Serial clock "L" pulse width	$t_{LSLH}$	SCK0 to SCK4		$4 t_{CP}$	—	ns	
SCK ↓ → SOT delay time	$t_{SLOV}$	SCK0 to SCK4, SOT0 to SOT4		—	150	ns	
Valid SIN → SCK ↑	$t_{VSH}$	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	
SCK ↑ → Valid SIN hold time	$t_{SHIX}$	SCK0 to SCK4, SIN0 to SIN4		60	—	ns	

- Notes :
- AC characteristic in CLK synchronized mode.
  - $C_L$  is load capacity value of pins when testing.
  - $t_{CP}$  is the machine cycle (Unit : ns) .

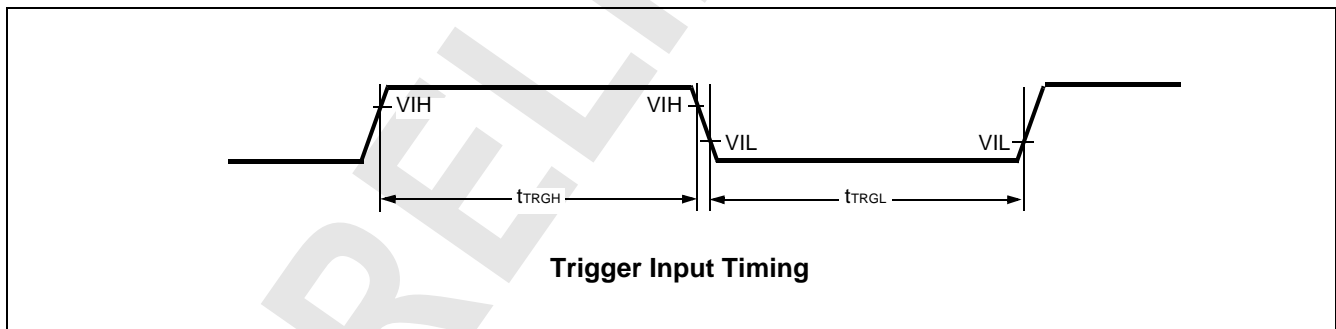




## (9) Trigger Input Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

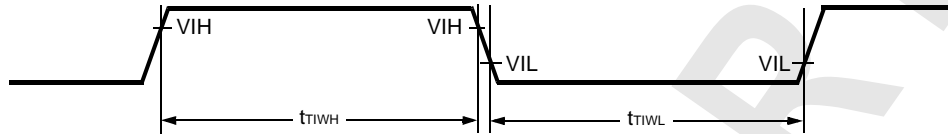
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TRGH}$ $t_{TRGL}$	INT0 to INT15, ADTG	—	$5 t_{CP}$	—	ns	



## (10) Timer Related Resource Input Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{r1WH}$	TIN0 to TIN3	—	4 $t_{CP}$	—	ns	
	$t_{r1WL}$	IN0 to IN7					

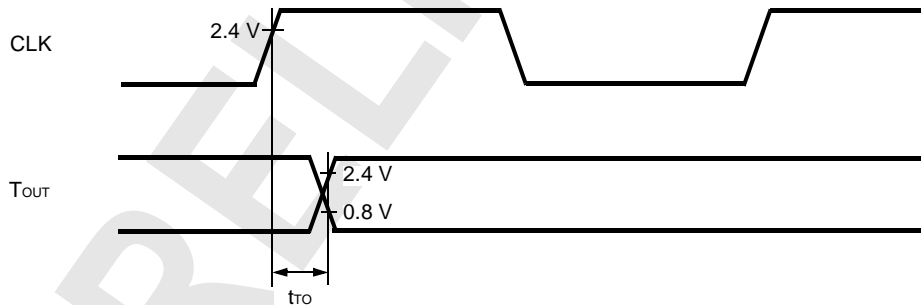


Timer Input Timing

## (11) Timer Related Resource Output Timing

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $V_{CC} = 4.5$  to  $5.5\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
$\text{CLK} \uparrow \Rightarrow T_{OUT}$ change time	$t_{ro}$	TOT0 to TOT3, PPG0 to PPGF	—	30	—	ns	



Timer Output Timing

# MB90340 Series

## 5. A/D Converter

( $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ ,  $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$ ,  $V_{CC} = \text{AV}_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = \text{AV}_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Conversion error	—	—	—	—	$\pm 3.0$	LSB	
Nonlinearity error	—	—	—	—	$\pm 2.5$	LSB	
Differential nonlinearity error	—	—	—	—	$\pm 1.9$	LSB	
Zero reading voltage	$V_{OT}$	AN0 to AN7	$\text{AVRL} - 1.5$	$\text{AVRL} + 0.5$	$\text{AVRL} + 2.5$	LSB	
Full scale reading voltage	$V_{FST}$	AN0 to AN7	$\text{AVRH} - 3.5$	$\text{AVRH} - 1.5$	$\text{AVRH} + 0.5$	LSB	
Conversion time	—	—	3.3	$66 t_{CP}$	—	$\mu\text{s}$	
Sampling time	—	—	1.6	$32 t_{CP}$	—	$\mu\text{s}$	
Analog port input current	$I_{AIN}$	AN0 to AN7	-5	—	+5	$\mu\text{A}$	
Analog input voltage range	$V_{AIN}$	AN0 to AN7	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	$\text{AVRL} + 2.7$	—	$\text{AV}_{CC}$	V	
	—	AVRL	0	—	$\text{AVRH} - 2.7$	V	
Power supply current	$I_A$	$\text{AV}_{CC}$	—	3.5	7.5	mA	
	$I_{AH}$	$\text{AV}_{CC}$	—	—	5	$\mu\text{A}$	*
Reference voltage current	$I_R$	AVRH	—	165	250	$\mu\text{A}$	
	$I_{RH}$	AVRH	—	—	5	$\mu\text{A}$	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

\* : When not operating A/D converter, this is the current ( $V_{CC} = \text{AV}_{CC} = \text{AVRH} = 5.0\text{ V}$ ) .

### Terminology

Conversion error : Absolute maximum conversion deviation with respect to the theoretical conversion line.

Nonlinearity : Relative maximum conversion deviation with respect to the theoretical conversion line connecting to the device unique zero reading voltage and full scale reading voltage.

Differential nonlinearity : Max conversion deviation in any two adjacent reading voltages with respect to the theoretical LSB conversion step.

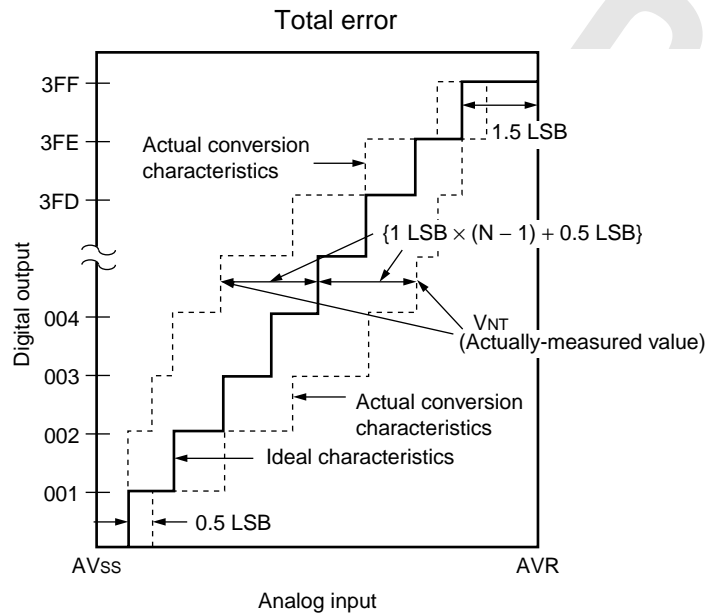
Zero reading voltage : Input voltage which results in the minimum conversion value.

Full scale reading voltage : Input voltage which results in the maximum conversion value.

- Notes :
- The accuracy gets worse as  $\text{AVRH} - \text{AVRL}$  becomes smaller.
  - Analog input external circuit output impedance should use the following conditions.  
External Circuit Output Impedance less than TBD k $\Omega$
  - If the external circuit output impedance is too high, there may insufficient time for sampling of the analog voltage.

## 6. Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linear error : Deviation between a line across zero-transition line (“00 0000 0000” ← → “00 0000 0001”) and full-scale transition line (“11 1111 1110” ← → “11 1111 1111”) and actual conversion characteristics.
- Differential linear error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error : Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB} = (\text{Ideal value}) \frac{AVR - AV_{SS}}{1024} \text{ [V]}$$

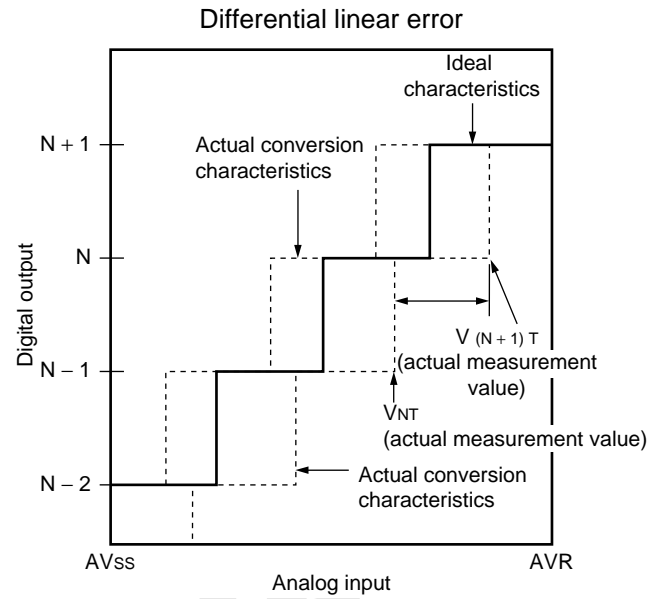
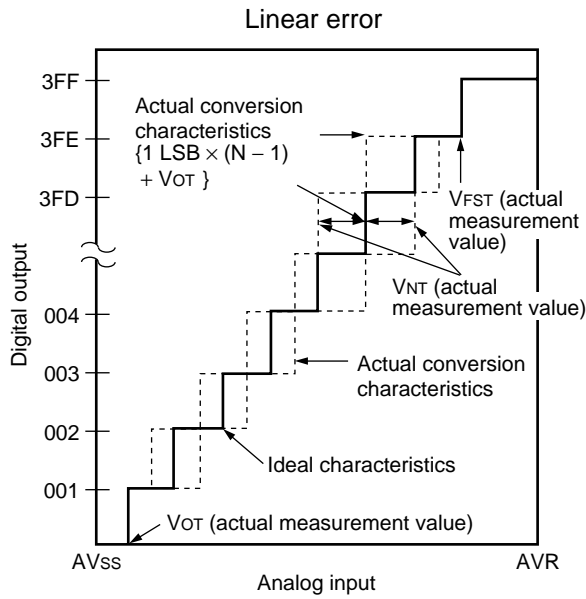
$$V_{OT} (\text{Ideal value}) = AV_{SS} + 0.5 \text{ LSB [V]}$$

$$V_{FST} (\text{Ideal value}) = AVR - 1.5 \text{ LSB [V]}$$

V<sub>NT</sub> : A voltage at which digital output transitions from (N - 1) to N.

(Continued)

(Continued)



$$\text{Linear error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$\text{Differential linear error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB} \quad [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \quad [\text{V}]$$

$V_{OT}$  : Voltage at which digital output transits from "000H" to "001H."

$V_{FST}$  : Voltage at which digital output transits from "3FEH" to "3FFH."

## 7. Notes on A/D Converter Section

Use the device with external circuits of the following output impedance for analog inputs :

Recommended output impedance of external circuits are :

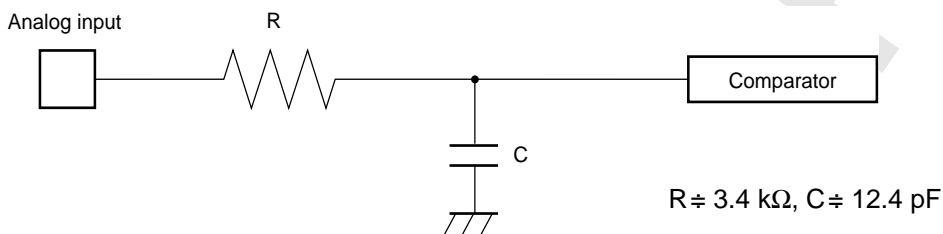
Approx.  $1.5\text{k}\Omega$  or lower ( $4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$ , sampling period  $\leq 0.5\ \mu\text{s}$ )

If the output impedance exceeds  $1.5\text{k}\Omega$ , set a longer sampling time or add an external capacitor compensate the the output impedance. About setting of sampling time, please refer to hardware manual of MB90340 series.

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model



Note : Use the values in the figure only as a guideline.

## 8. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25\text{ }^\circ\text{C}$ $V_{CC} = 5.0\text{ V}$	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16 bit width) programming time		—	16	3,600	$\mu\text{s}$	Except for the over head time of the system
Programs/Erase cycle	—	10,000	—	—	cycle	

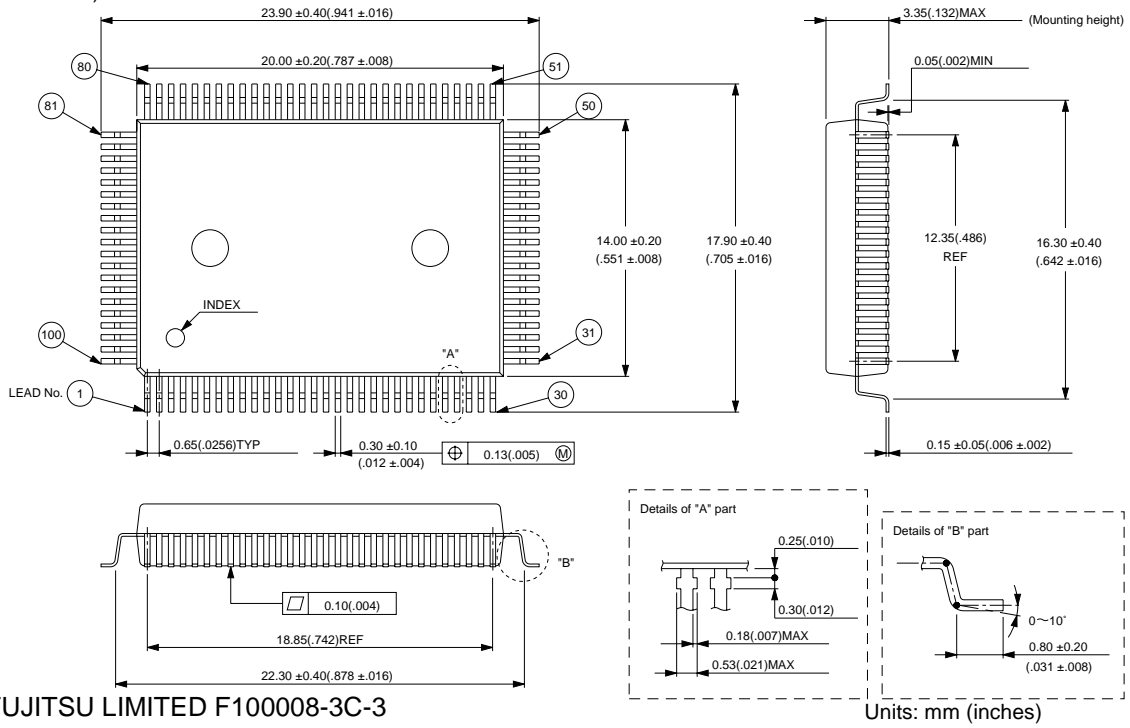
# MB90340 Series

## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F347PF	100-pin Plastic QFP (FPT-100P-M06)	under development
MB90F347SPF		
MB90F347CPF		
MB90F347CSPF		
MB90F347PFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90F347SPFV		
MB90F347CPFV		
MB90F347CSPFV		
MB90V340	299-pin Ceramic PGA (PGA-299C-A01)	For evaluation, under development

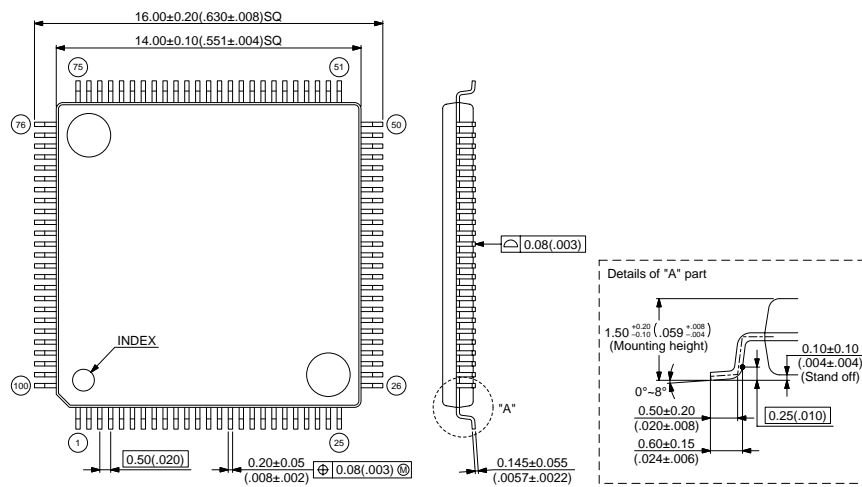
## 1. PACKAGE DIMENSION

Plastic QFP, 100 pins  
(FPT-100P-M06)



100-pin Plastic LQFP  
(FPT-100P-M05)

\*Pins width and pins thickness include plating thickness.



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