



Corrections of Hardware Manual

MB90390

hm90390-cm44-10122-1e-corr-x1-03

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Addendum, MB90390 Hardware Manual (CM44-10122-1E)

This is the Addendum for the Hardware Manual CM44-10122-1E of the MB90390 microcontroller series. It describes all known discrepancies of the MB90390 microcontroller series Hardware Manual.

Ref. Number (Internal ref. number) (Text Link)	Date dd.mm.yy	Version No.	Chapter/Page	Description/Correction
HWM90390001	10.03.03	1.00		Transition to standby mode, Standby Cancel failure behavior added
HWM90390002	26.05.03	1.01	13.1/182 13.3/186	16bit free running timer, typos
HWM90390003	15.08.03	1.02		ROM Correction Register
HWM90390003	18.08.03	1.03		ROM Correction Register, description corrected

HWM90390001 Transition to standby mode

The definition of Standby Cancel Failure is that the CPU will execute wrong instructions when an interrupt is executed during transition to Standby mode *0 at a certain time. Fujitsu can reproduce this phenomenon Fujitsu internally and has found the cause.

*0:Definition of Standby mode
Main sleep mode, PLL sleep mode, Sub-sleep mode
Time base timer mode, Watch mode, Main watch mode
Main stop mode, PLL stop mode, Sub-stop mode
*Main watch mode is only for MB90370 series.

In the following cases, no problem occurs:
-Standby mode is not used
-Standby mode is released only by external reset

For further information refer to 'F2MC16-LX Standby Cancel Failure' document.

HWM90390002 16bit free running timer, typos

The free running timers in MB90390 contain 3 control bits for count clock selection CLK[2:0]. By mistake, only two count clock selection bits CLK[1:0] are described in the following parts of the Hardware Manual:

chapter 13.1, page: 182

- 16-bit-free-running timer

wrong:

- **Four** counter clocks are available.
Internal clock: $\phi/4$, $\phi/16$, $\phi/64$, $\phi/256$

correct:

- **Eight** counter clocks are available.
Internal clock: ϕ , $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$

chapter 13.3, page 186

- 16-bit free runing timer block diagram

wrong:

Figure 13.3-1



correct:

Figure 13.3-1



HWM90390003

ROM Correction address

The Address of Rom correction has changed

Devices	Address Range	Remarks
MB90V390	A	
MB90V390H	B	
MB90F394H	A	Date Code: =< 0228 xxx; 0229 K12
MB90F394H	B	Date Code: 0229 K11; >= 0230 xxx

Description:

Address Range	
A	ROM correction 0 address registers start at 001FF0h (in RAM area)
B	ROM correction 0 address registers start at 0035E0h (outside RAM area)