FUJITSU

Corrections of Hardware Manual

MB90385 -

hm90385-cm44-10118-1e-corr-x1-01

Addendum, MB90385 Hardware Manual (CM44-10118-1E)

This is the Addendum for the Hardware Manual CM44-10118-1E of the MB90385 microcontroller series. It describes all known discrepancies of the MB90385 microcontroller series Hardware Manual.

Ref. Number (Internal ref. number) (Text Link)	**Date** dd.mm.yy	**Version No.**	**Chapter/Page**	**Description/Correction**
HWM90385001	07.01.03	1.00	19	CAN, 'Hit and Away' description added
HWM90385002	07.01.03	1.00		Transition to standby mode, Standby Cancel failure behavior added
HWM90385003	19.04.04	1.01	1.6	Pin Description corrected
HWM90385004	19.04.04	1.01	3.1.2	Memory Map corrected
HWM90385005	19.04.04	1.01	3.6.1	Reset Factors and Oscillation Stabilization Wait Time, Figure corrected
HWM90385006	19.04.04	1.01	3.7.4	Clock Mode, typos corrected
HWM90385007	19.04.04	1.01	3.8	Low-power Consumption Mode, Note added
HWM90385008	19.04.04	1.01	3.8.3	Low-power Consumption Mode Control Register (LPMCR), Note corrected
HWM90385009	19.04.04	1.01	3.8.6	State Transition in Standby Mode, Note corrected

Ref. Number (Internal ref. number) (Text Link)	**Date** dd.mm.yy	**Version No.**	**Chapter/Page**	**Description/Correction**
HWM90385010	19.04.04	1.01	3.8.8	Precautions when Using Low-power Consumption Mode, typos corrected
HWM90385011	19.04.04	1.01	3.9.2	Mode Data, typos corrected
HWM90385012	19.04.04	1.01	8.3.2	Timer Control Status Registers (Low), typos corrected
HWM90385013	19.04.04	1.01	9.1	Overview of Watch Timer, typos corrected
HWM90385014	19.04.04	1.01	9.2	Block Diagram of Watch Timer, Figure corrected
HWM90385015	19.04.04	1.01	9.3.1	Watch Timer Control Register (WTC), Table corrected
HWM90385016	19.04.04	1.01	9.5	Explanation of Operation of Watch Timer, typos corrected
HWM90385017	19.04.04	1.01	12.5	Precautions when Using DTP/External Interrupt, typos corrected
HWM90385018	19.04.04	1.01	13.1	Overview of 8-/10-bit A/D Converter, Table corrected
HWM90385019	19.04.04	1.01	15.3.1	Control Status Register (High) (CSR: H), Note corrected
HWM90385020	19.04.04	1.01	15.3.2	Control Status Register (Low) (CSR: L), Note corrected

Chapter 15. CAN Controller

'Hit and Away' description:

Affected Parts: MB90V495G, MB90F387/S, MB90387/S

Caution for disabling Message Buffers by BVAL bits

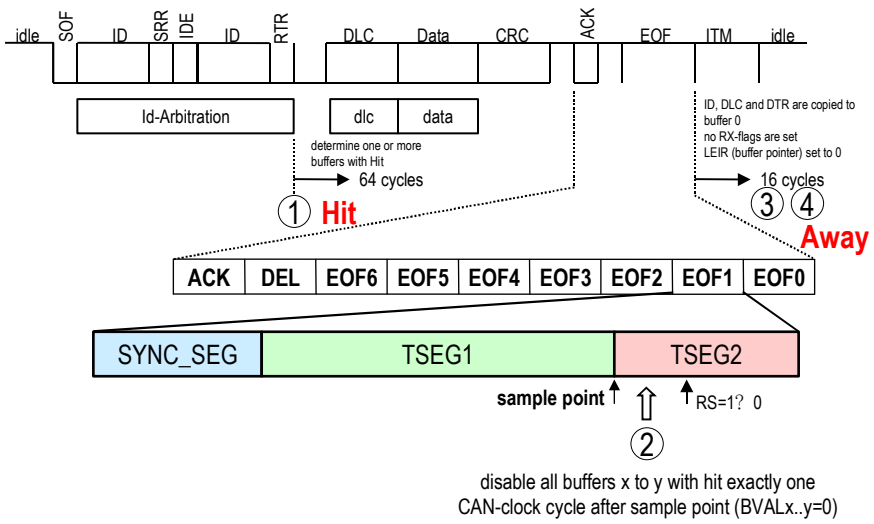
1 Caution for Reception

1.1 Behaviour

If there is a complete (no error until 6th bit of EOF) incoming message that have passed the acceptance filter, then this message is stored into a message buffer x (with x=0…15). If this store operation coincides with reset operation of the corresponding BVAL bit (BVALx=0), the received message will be stored into the message buffer 0 regardless of register settings. Note that this coincidence has to happen within a specific CAN-clock cycle (see event 2 in figures). Hence, the probability is very low.
If transmission request of buffer 0 is set (TREQ0=1), the above-mentioned behaviour will lead to the following transmission of a message. This message consists of the received ID, DLC and Data together with original IDE and RTR bits set of the message buffer 0.
However, if there are two or more message buffers with passing acceptance filers for the incoming message and only buffer x is disabled, the message will be stored into the 2nd prioritised message buffer.
If there are two or more message buffers with passing acceptance filers for the incoming message and all those buffers are disabled, the message will be stored into buffer 0.

1.2 Operation to avoid

When disabling message buffers by the BVAL register, it must be avoided that the write operation to the BVAL register coincides with the store operation of the received message in the CAN Controller.
The following diagram illustrates the timing to be avoided for the BVAL write operation.



① CAN-controller determines buffers, which can store the message, because their acceptance filters had been passed.

② Software disable all buffers with hit exactly one CAN-clock cycle after the sample point of EOF1.

③ CAN-controller stores received ID, DLC and data in buffer 0 regardless of the buffers determined in ①.

④ CAN-Controller sets LEIR to point to buffer 0 but RX-flags (RCR, ROVR, RRTRR) are not set.

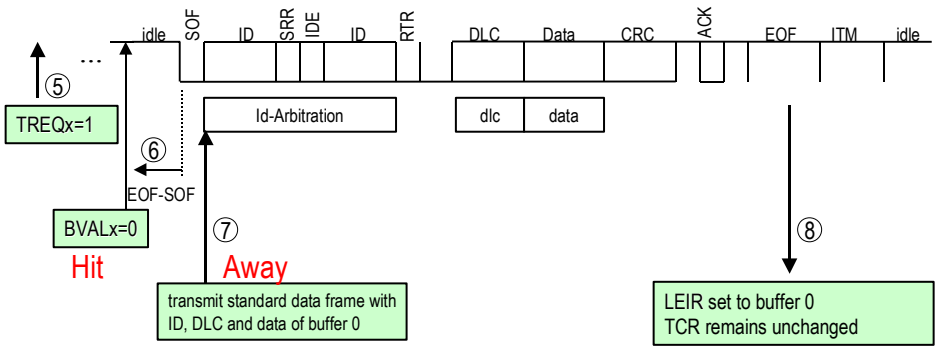
2. Caution for Transmission

2.1 Behaviour

When there is a pending transmission of buffer x and the CAN bus status is in Intermission or in Bus Idle, the CAN-controller will load the message from buffer x in order to send it. If this load operation coincides with disabling the pending message buffer x by clearing the BVAL bit, this results in transmission of a Standard message. This message consists of RTR=0, IDE=0, DLC, 11 ID bits and Data stored in the message buffer 0.
Note that this coincidence has to happen with in a specific CAN-clock cycle. Hence, the probability is very low. The position of that cycle depends also on previous frame reception and occurrence of error frames.

2.2 Operation to avoid

When disabling message buffers by the BVAL register, it must be avoided that the write operation to the BVAL register coincides with the preparation for the next transmission in the CAN Controller.
The following diagram illustrates the timing to be avoided for the BVAL write operation.



⑤ Software requests transmission of buffer x by setting TREQx.
⑥ Software disables the buffer x by clearing BVALx.
⑦ CAN-controller transmits a standard data frame with ID, length code and data of buffer 0.
⑧ After completion of frame only LEIR is updated for buffer 0. However, TCR is not set (neither for buffer 0 nor for buffer x).

3. Correct Operation

3.1 Operation for re-configuring receive message buffers

Depending on CAN applications, it may be necessary to re-configure message buffers after receiving messages through the already active CAN communication. While the CAN bus is active, it is necessary to follow one of the two operations described below to re-configure message buffers by ID, AMS and AMR0/1 register settings. "Active" means that read value of the HALT bit is 0 and the CAN Controller is ready to receive and transmit messages.

1.1.1 Use of HALT bit

Write 1 to the HALT bit and read it back for checking the result is 1. Then change settings for the ID/AMS/AMR0/1 registers.

1.1.2 No use of Message Buffer 0

Do not use the message buffer 0. In other words, disable message buffer (BVAL=0), prohibit receive interrupt (RIE=0) and do not request transmission (TREQ=0).

3.2 Operation for processing received message.

When reading a received message from a message buffer, consideration must be given for possible over-write operation by next incoming messages. Disabling receive operation by the BVAL bit must not be used for this purpose. Use the ROVR bit for checking, if over-writing has been performed. For details, refer to description of ROVR in the hardware manual.

3.3 Cancellation of transmission request

Do not use the BVAL bit for suppressing/cancellation of transmission request. The TCANR bit is prepared for this purpose.

3.4 Composing transmission message

When composing a transmission message by writing to ID, data and other registers, the message buffer should be disabled by the BVAL bit.
In this case, the BVAL bit should reset (BVAL=0) after checking if the TREQ bit is 0 or after completion of the previous message transmission (TC=1).

4. Example of avoiding Hit-And-Away

1. Do not use message buffer 0. Keep it always disabled (BVAL0 = 0).
By not using buffer 0 the processing of wrongly received messages in buffer 0 is avoided. Even if data are received in this buffer, they have no influence.
2. Set an unused 11-Bit identifier in buffer 0.
"Unused" means that the identifier has no meaning to any node in the network. If an invalid standard data frame is sent according to the condition described in "0
2. Caution for Transmission", that frame must not cause misoperation of other nodes.
3. Use overrun test while processing a received message.
After temporarily saving received message, test for overrun (ROVRR). If overrun occurred, read the buffer again, because the read data before overrun could be inconsistent.
4. Wait for completion of transmission.
A buffer must not be disabled by clearing the BVAL-flag, as long as there is a pending transmission. Easiest way to wait for transmission completion is to use transmission interrupt but polling of TREQ is also possible.

Transition to standby mode

The definition of Standby Cancel Failure is that the CPU will execute wrong instructions when an interrupt is executed during transition to Standby mode *0 at a certain time. Fujitsu can reproduce this phenomenon Fujitsu internally and has found the cause.

*0:Definition of Standby mode
Main sleep mode, PLL sleep mode, Sub-sleep mode
Time base timer mode, Watch mode, Main watch mode
Main stop mode, PLL stop mode, Sub-stop mode
*Main watch mode is only for MB90370 series.

In the following cases, no problem occurs:
-Standby mode is not used
-Standby mode is released only by external reset

For further information refer to 'F2MC16-LX Standby Cancel Failure' document.

Chapter 1.6 Pin Description

Table 1.6-1 was corrected as indicated by shading below.

• error

Pin No. M06	Pin Name	Circuit Type	Function
46	X0A*	A	Low-speed oscillation pin.
	P35*		General-purpose I/O port.
47	P35*	A	Low-speed oscillation pin.
	P36*		General-purpose I/O port.

• Correct

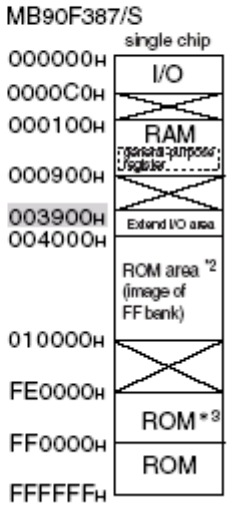
Pin No. M06	Pin Name	Circuit Type	Function
46	X0A*	A	Low-speed oscillation pin.
	P35*	D	General-purpose I/O port.
47	P35*	A	Low-speed oscillation pin.
	P36*	D	General-purpose I/O port.

Chapter 3.1.2 Memory Map

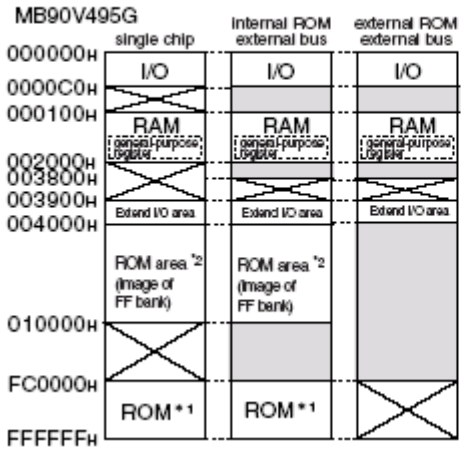
Figure 3.1-3 was corrected as indicated by shading below.

• Error

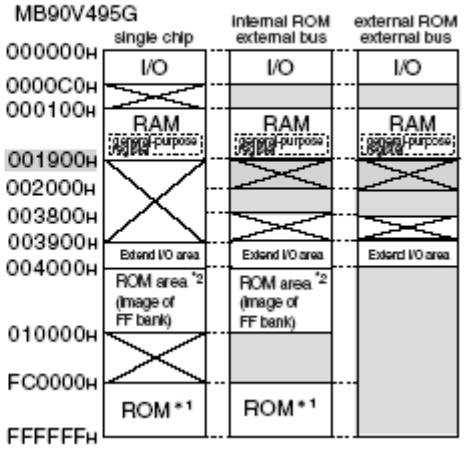
• Correct



• Error



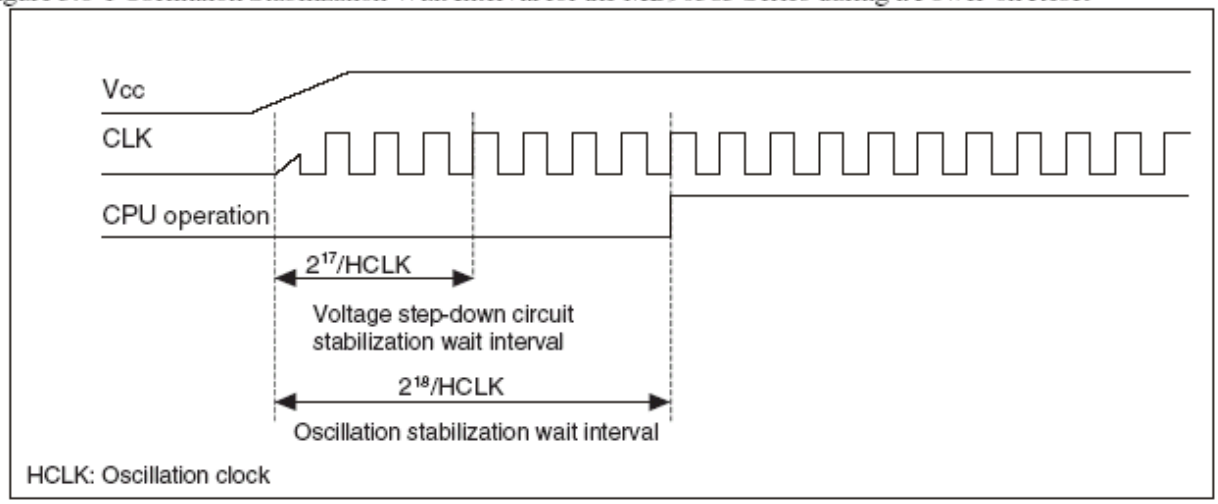
• Correct



Chapter 3.6.1 Reset Factors and Oscillation Stabilization Wait Time

Figure 3.6-1 was moved next Table 3.6-2.

Figure 3.6-1 Oscillation Stabilization Wait Interval for the MB90385 Series during a Power-on Reset



HWM90385006

Chapter 3.7.4 Clock Mode

The following sentence of "Transition from main clock mode to subclock mode" in "Transition of Clock
Mode" was corrected as indicated by shading below.
• Error
When the edge of the subclock is detected
• Correct
synchronizing the subclock (approx. 130µs).

Notes of "Machine Clock" were added as indicated by the shading below:

• When transiting a clock mode, do not transit a clock mode to any other clock mode or a low-power consumption mode until the completion of transition. Reference the MCM and SCM bits in the clock select register (CKSCR) to check that the transition of a clock mode is completed. If the mode is switched to another clock mode or low-power-consumption mode before completion of switching, the mode may not be switched.

The explanation of (9) in Figure 3.7-5 was corrected as indicated by the shading blow:
• Error
(9) Subclock oscillation stabilization wait time termination (2^{15}/SCLK max.)
• Correct
(9) Subclock oscillation stabilization wait time termination (2^{14}/SCLK)

Chapter 3.8 Low-power Consumption Mode

Note of "Stop Mode" were added as indicated by the shading below:
• When transiting a clock mode, do not transit a clock mode to any other clock mode or a low-power consumption mode until the completion of transition. Reference the MCM and SCM bits in the clock select register (CKSCR) to check that the transition of a clock mode is completed. If the mode is switched to another clock mode or low-power-consumption mode before completion of switching, the mode may not be switched.

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Chapter 3.8.3 Low-power Consumption Mode Control Register (LPMCR)

Note of "■ Low-Power Consumption Mode Control Register (LPMCR)" was corrected as indicated by the shading blow:

Notes: • When transiting to a low-power consumption mode using the low-power consumption mode control register (LPMCR), use the instructions listed in Table 3.8-2 "Instructions at Transition to Low-power Consumption Mode".

• The low-power consumption mode transition instruction in table 3.8-2 must always be followed by an array of instructions highlighted by a dotted line below.

```
MOV    LPMCR,#H'XX  ; the low-power consumption mode transition instruction in table 3.8-2
NOP
NOP
JMP    $+3          ; jump to next instruction
MOV    A,#H'10      ; any instruction
```

The devices do not guarantee its operation after returning from the standby mode if you place an array of instructions other than the one enclosed in the dotted line.

• To access the low-power consumption mode control register (LPMCR) with C language, refer to "• Notes on Accessing the Low-Power Consumption Mode Control Register (LPMCR) to Enter the Standby Mode" in the section 3.8.8 "Notes on Using the Low-Power Consumption Mode".

• When word-length is used for writing the low-power consumption mode control register, even addresses must be used. Using odd addresses to switch to a low-power consumption mode may result in a malfunction.

• To set a pin to high impedance when the pin is shared by a peripheral function and a port in stop mode, watch mode or timebase timer mode, disable the output of peripheral functions, and set the STP bit of the low-power consumption mode control register (LPMCR) to 1 or set the TMD bit to 0. This applies to the following pins:
P14/PPGO, P15/PPG1, P16/PPG2, P17/PPG3, P21/TOT0, P23/TOT1

• There is no sub-clock in MB90F387S and MB90387S.

The shading in the table below indicates changes made to Table 3.8 –2.

MOV io,#imm8	MOV dir,#imm8	MOV eam,#imm8	MOV eam,Ri
MOV io,A	MOV dir,A	MOV addr16,A	MOV eam,A
MOV @RLi+disp8,A			
MOVW io,#imm16	MOVW dir,#imm16	MOVW eam,#imm16	MOVW eam,RWi
MOVW io,A	MOVW dir,A	MOVW addr16,A	MOVW eam,A
MOVW @RLi+disp8,A			
SETB io:bp	SETB dir:bp	SETB addr16:bp	
CLRB io:bp	CLRB dir:bp	CLRB addr16:bp	

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Chapter 3.8.6 State Transition in Standby Mode

Note of "State Transition Diagram" was corrected as indicated by the shading below:
•In attempting to switch the clock mode, do not attempt to switch to another clock mode or low-power consumption mode until the first switching is completed. The MCM and SCM bits of the clock selection register (CKSCR) indicate that switching is completed. If the mode is switched to another clock mode or low-power-consumption mode before completion of switching, the mode may not be switched.

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Chapter 3.8.8 Precautions when Using Low-power Consumption Mode

The following sentence of "□ Oscillation stabilization wait time of subclock" in "Oscillation Stabilization Wait Time" was corrected as indicated by shading below.
• Error
…… The oscillation stabilization wait time of subclock is fixed at 2^{15}/SCLK (SCLK: subclock).
• Correct
…… The oscillation stabilization wait time of subclock is fixed at 2^{14}/SCLK (SCLK: subclock).

The following description was added to "Transition of Clock Mode".
…… Reference the MCM and SCM bits in the clock select register (CKSCR) to check that the transition of a clock mode is completed. If the mode is switched to another clock mode or low-power-consumption mode before completion of switching, the mode may not be switched.

The following description was added to "3.8.8 Precautions when Using Low-power Consumption Mode".
□ Notes on Accessing the Low-Power Consumption Mode Control Register (LPMCR) to Enter the Standby Mode
• To access the low-power consumption mode control register (LPMCR) with assembler language
- To set the low-power consumption mode control register (LPMCR) to enter the standby mode, use the instruction listed in Table 3.8-2.

- The low-power consumption mode transition instruction in table 3.8-2 must always be followed by an array of instructions highlighted by a dotted line below.

```
MOV    LPMCR,#H'xx  ; the low-power consumption mode transition instruction in table 3.8 –2
NOP
NOP
JMP    $+3          ; jump to next instruction
MOV    A,#H'10      ; any instruction
```

The devices does not guarantee its operation after returning from the standby mode if you place an array of instructions other than the one enclosed in the dotted line.

• To access the low-power consumption mode (LPMCR) with C language

To enter the standby mode using the low-power consumption mode control register (LPMCR), use one of the following methods (1) to (3) to access the register:

(1) Specify the standby mode transition instruction as a function and insert two_wait_nop() built-in functions after that instruction. If any interrupt other than the interrupt to return from the standby mode can occur within the function, optimize the function during compilation to suppress the LINK and UNLINK instructions from occurring.

Example: Watch mode or timebase timer mode transition function

```
void enter_watch(){
IO_LPMCR.byte = 0x10; /* Set LPMCR TMD bit to "0" */
_wait_nop();
_wait_nop();
}
```

(2) Define the standby mode transition instruction using _asm statements and insert two NOP and JMP instructions after that instruction.

Example: Transition to sleep mode

```
_asm(" MOVI: _IO_LPMCR,#H'58); /* Set LPMCR SLP bit to "1" */
_asm(" NOP");
_asm(" NOP");
_asm(" JMP $+3"); /* Jump to next instruction */
```

(3) Define the standby mode transition instruction between #pragma asm and #pragma endasm and insert two NOP and JMP instructions after that instruction.

Example: Transition to stop mode

```
#pragma asm
MOV I: _IO_LPMCR,#H'98 /* Set LPMCR STP bit to "1" */
NOP
NOP
JMP $+3 /* Jump to next instruction */
#pragma endasm
```

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Chapter 3.9.2 Mode Data

The following figure title was corrected as indicated by shading below.
• Error
Figure 3.9-2 Mode Data (TBTC)
• Correct
Figure 3.9-2 Mode Data

HWM90385012 TOP

Chapter 8.3.2 Timer Control Status Registers (Low) (TMCSR0: L, TMCSR1: L)

The following sentence of bit 0 in Table 8.3-3 was corrected as indicated by the shading below:
• Error ……
Read: 1 is always read.
• Correct ……
Read: 0 is always read.

HWM90385013 TOP

Chapter 9.1 Overview of Watch Timer

The following sentence of "□ Interval Timer Function" was corrected as indicated by the shading below:
• Error
  • The interval time of the watch timer can be selected from seven types shown in Table 9.1-1 "Interval Times of Watch Timer".
• Correct
  • The interval time of the watch timer can be selected from 8 types shown in Table 9.1-1 "Interval Times of Watch Timer".

Table 9.1-1 was corrected as indicated by the shading below:

• Error

Subclock Cycle	Interval Time
SCLK (122 µs)	2^8/SCLK (31.25 ms)
	2^9/SCLK (62.5 ms)
	2^{10}/SCLK (125 ms)
	2^{11}/SCLK (250 ms)
	2^{12}/SCLK (500 ms)
	2^{13}/SCLK (1.0 s)
	2^{14}/SCLK (2.0 s)
	2^{15}/SCLK (4.0 s)

• Correct

Subclock Cycle	Interval Time
SCLK (122 µs)	2^8/SCLK (31.25 ms)
	2^9/SCLK (62.5 ms)
	2^{10}/SCLK (125 ms)
	2^{11}/SCLK (250 ms)
	2^{12}/SCLK (500 ms)
	2^{13}/SCLK (1.0 s)
	2^{14}/SCLK (2.0 s)
	2^{15}/SCLK (4.0 s)

Table 9.1-2 was corrected as indicated by the shading below:

• Error

Where to Supply Clock	Clock Cycle
Timer for oscillation stabilization wait time of subclock	2^{15}/SCLK (4.000 s)
Watchdog timer	2^{10}/SCLK (125 ms)
	• • •

• Correct

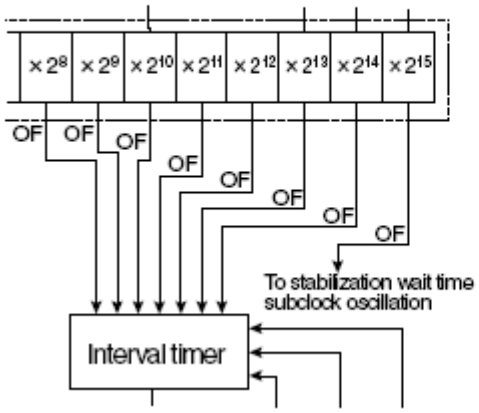
Where to Supply Clock	Clock Cycle
Timer for oscillation stabilization wait time of subclock	2^{14}/SCLK (2.000 s)
Watchdog timer	2^{10}/SCLK (125 ms)
	• • •

HWM90385014 TOP

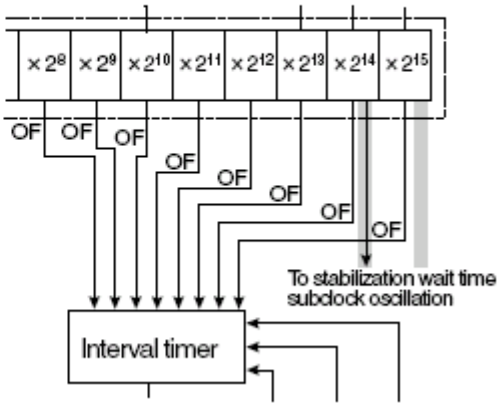
Chapter 9.2 Block Diagram of Watch Timer

"Figure 9.2-1 Block Diagram of Watch Timer" was corrected as indicated by the shading below:

• Error



• Correct



Chapter 9.3.1 Watch Timer Control Register (WTC)

The following sentence of bit 6 in Table 9.3-1 was corrected as indicated by the shading below:

• Error

Bit Name		Function
•••	•••	•••
bit 6	SCE: Oscillation stabilization wait time end bit	..... • The oscillation stabilization wait time of the subclock is fixed at 2^{15}/SCLK (SCLK: subclock frequency).
•••	•••	•••

• Correct

Bit Name		Function
•••	•••	•••
bit 6	SCE: Oscillation stabilization wait time end bit	..... • The oscillation stabilization wait time of the subclock is fixed at 2^{14}/SCLK (SCLK: subclock frequency).
•••	•••	•••

Chapter 9.5 Explanation of Operation of Watch Timer

The following sentence of "Oscillation Stabilization Wait Time Timer of Subclock" was corrected as indicated by the shading below:

• Error
  • The subclock oscillation stabilization wait time is fixed at 2^{15}/SCLK (SCLK: subclock frequency).

• Correct
  • The subclock oscillation stabilization wait time is fixed at 2^{14}/SCLK (SCLK: subclock frequency).

Chapter 12.5 Precautions when Using DTP/External Interrupt

The following sentence of "□ External interrupt input polarity" in "□ Precautions when Using DTP/External
Interrupt Circuit" was corrected as indicated by the shading below:

……

• When a level causing an interrupt factor is input with level detection set in the detection level setting register, the interrupt request flag bit (EIRR:ER) of the DTP/external interrupt factor register is set to 1 and the factor is held as shown in Figure 12.5-1 "Clearing Interrupt Request Flag Bit (EIRR:ER) when Level Set".
With the factor held in the interrupt request flag bit (EIRR:ER), the request to the interrupt controller remains active if the interrupt request is enabled (ENIR: EN = 1) even after the DTP/external interrupt factor is cancelled. To cancel the request to the interrupt controller, clear the interrupt request

flag bit (EIRR:ER) as shown in Figure 12.5-2 "DTP/External Interrupt Factor and Interrupt Request Generated when Interrupt Request Enabled".

Figure 12.5-1 Clearing Interrupt Request Flag Bit (EIRR: ER) when Level Set

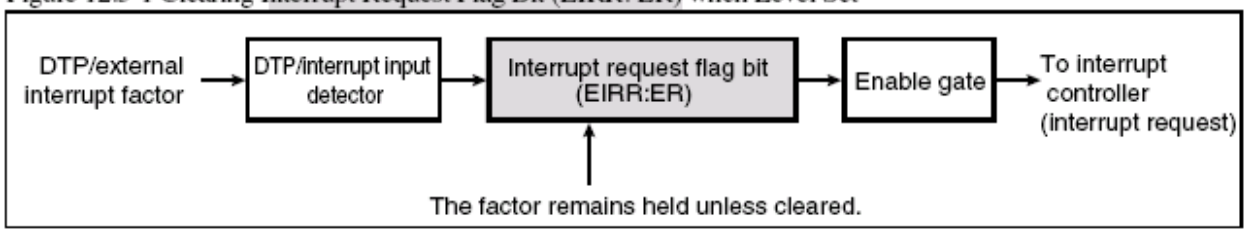
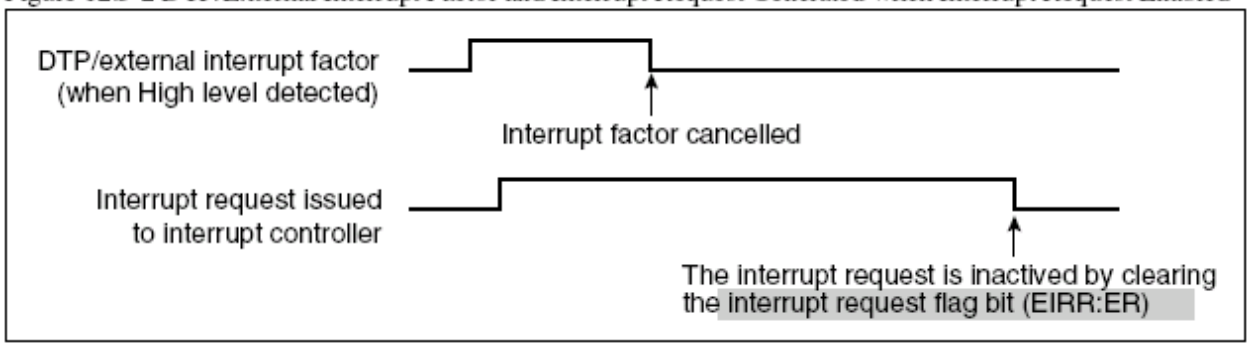


Figure 12.5-2 DTP/External Interrupt Factor and Interrupt Request Generated when Interrupt Request Enabled



HWM90385018 TOP

Chapter 13.1 Overview of 8-/10-bit A/D Converter

The following sentence as indicated by the shading was added to the function of bit 9 in Table 13.3-2:

Bit Name		Function
• • •	• • •	• • •
bit 9	STRT: A/D conversion software start bit	..... When set to 0: Invalid. The state remains unchanged. Read: The byte/word command reads "1". The read-modify-write series commands read "0". Note: .....

The following sentences of bit 3 to bit 5 in "Table 13.3-3 were corrected as indicated by the shading below:

Bit Name		Function
•••	•••	•••
bit 3 to bit 5	ANS2 to ANS0: A/D conversion start channel select bits	These bits set the channel at which A/D conversion start. At read, the channel number under A/D conversion or A/D-converted immediately before A/D conversion pauses can be checked. And before A/D conversion starts, the previous conversion channel will be read even if these bits have already been set to the new value. These bits are initialized to "000_B" at reset. ••• Read (During A/D conversion): The channel numbers (7 to 0) under A/D conversion are read. Read (During pause-conversion mode and temporary stop): At read during a pause, the channel number A/D-converted immediately before a pause is read. Note: Do not set the A/D conversion start channel bits (ANS2 to ANS0) during A/D conversion.

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Chapter 15.3.1 Control Status Register (High) (CSR: H)

The Note of "Control Status Register (High) (CSR: H)" was corrected as indicated by the shading below:

Note: It is prohibited to execute a bit operation (read-modify-write) instruction on the lower 8 bits of control status register (CSR). Only in the case of HALT bits unchanged, use any bit operation instructions without problems (initialization of the macro instructions, etc.).

HWM90385020 TOP

Chapter 15.3.2 Control Status Register (Low) (CSR: L)

The Note of "Control Status Register (Low) (CSR: L)" was corrected as indicated by the shading below:

Note: It is prohibited to execute a bit operation (read-modify-write) instruction on the lower 8 bits of control status register (CSR). Only in the case of HALT bits unchanged, use any bit operation instructions without problems (initialization of the macro instructions, etc.).