

This errata sheet describes the functional deviations known at the release date of this document.

Errata History

Lot Number	Trouble list	Status
All	T01, T02, T03, T04, T05, T06, T07, T08, T09, T10, T11, T12, T13	Not Fixed

Trouble descriptions

T01	During UART reception, clearing REN may generate unexpected IT.
Description	During Uart reception, if the REN bit is cleared between a start bit detection and the end of reception, the Uart will not discard the data (RI is set).
Workaround	Test REN at the beginning of Interrupt routine just after CLR RI, and to run the Interrupt routine code only if REN is set.

T02	Double IT on external falling edge on INT1 or INT0 in X2 Mode
Description	When CPU is in X2 mode and Timer1 or Timer 0 in X1 mode (CKCON = 0x7F), IEx flag is not cleared by hardware after servicing interrupt. In this case, the CPU executes the ISR a second time.
Workaround	The work around is to clear IEx bit in Interrupt subroutine. INT1_ISR : ; Interrupt sub routine CLR IE1

T03	Internal Resistor on Reset Pin
Description	Deviation from electrical specification. Typical value for internal resistor on Reset pin: 20K Ohms
Workaround	No



80C51 MCUs

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T04	Bootloader - Write Page API - V1.1
Description	The Write Page API does not work correctly with the full page size.
Workaround	Write by 32 bytes size page instead of 128 bytes.

T05	Bootloader - Read Philips compatibility - V1.1.
Description	The previous version added FF bytes after the last address to complete the last 16 bytes line.
Workaround	Ignore the returned data above the end address of the Read command.

T06	Bootloader - SBV and BSB protection - V1.1
Description	SBV and BSB are not protected with SSB.
Workaround	No

T07	Bootloader - Program Byte API - V1.1
Description	No returned value Acc=00h if programming OK.
Workaround	No

T08	Bootloader - Write SSB level 0 - V1.1
Description	The command "Write SSB level0" is allowed in level 1 security. So the device can be unprotected.
Workaround	No

T09	SPI interface - Transmission on Master Mode
Description	A 9th bit is transmitted by the interface when the clock rate is set on divide by 2 mode and a positive polarity is selected ; the SPR2, SPR1, SPR0 bits are cleared (000) and CPOL = 1 on the SPCON register.
Workaround	Set the clock rate divide by 4 and X2 mode.

T10	SPI interface - Spi SS pin Limitation on Master/Slave
Description	The SS pin of the Spi was not got back as an I/O when a One-to-One Master/Slave intercommunication is performed.
Workaround	No

T11	Movc instruction on boot memory from boot memory does'nt work
Description	No movc instruction is performed when a program running on the boot memory try to read is own code by the movc instruction
Workaround	No

T12	Power On Flag
Description	Power On Flag doesn't work.
Workaround	No

T13	SPI - Spi Slave Responding in a Multislave configuration when not selected by the Master and its SPDAT register loaded
Description	In a multislave configuration, if the master is sending the Sck and the Tx data to all the slaves, and only one slave is selected, the non-selected slaves respond and generate the end of the transmission interruption (SPIF) if their SPDAT registers are loaded before the transmission.
Workaround	No

T14	SPI - Spi Slave not responding when selected and not loaded
Description	SPI Slave not responding when selected by a Master and no Data is loaded to be transmitted. No Rx data is registered and no SPIF interruption is generated at the end of the Trans
Workaround	No



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